MN1-S001

VERSION 1

SSC-210 VET

SERVICE MANUAL

SHANGHAI ALOKA MEDICAL EQUIPMENT CO.,LTD

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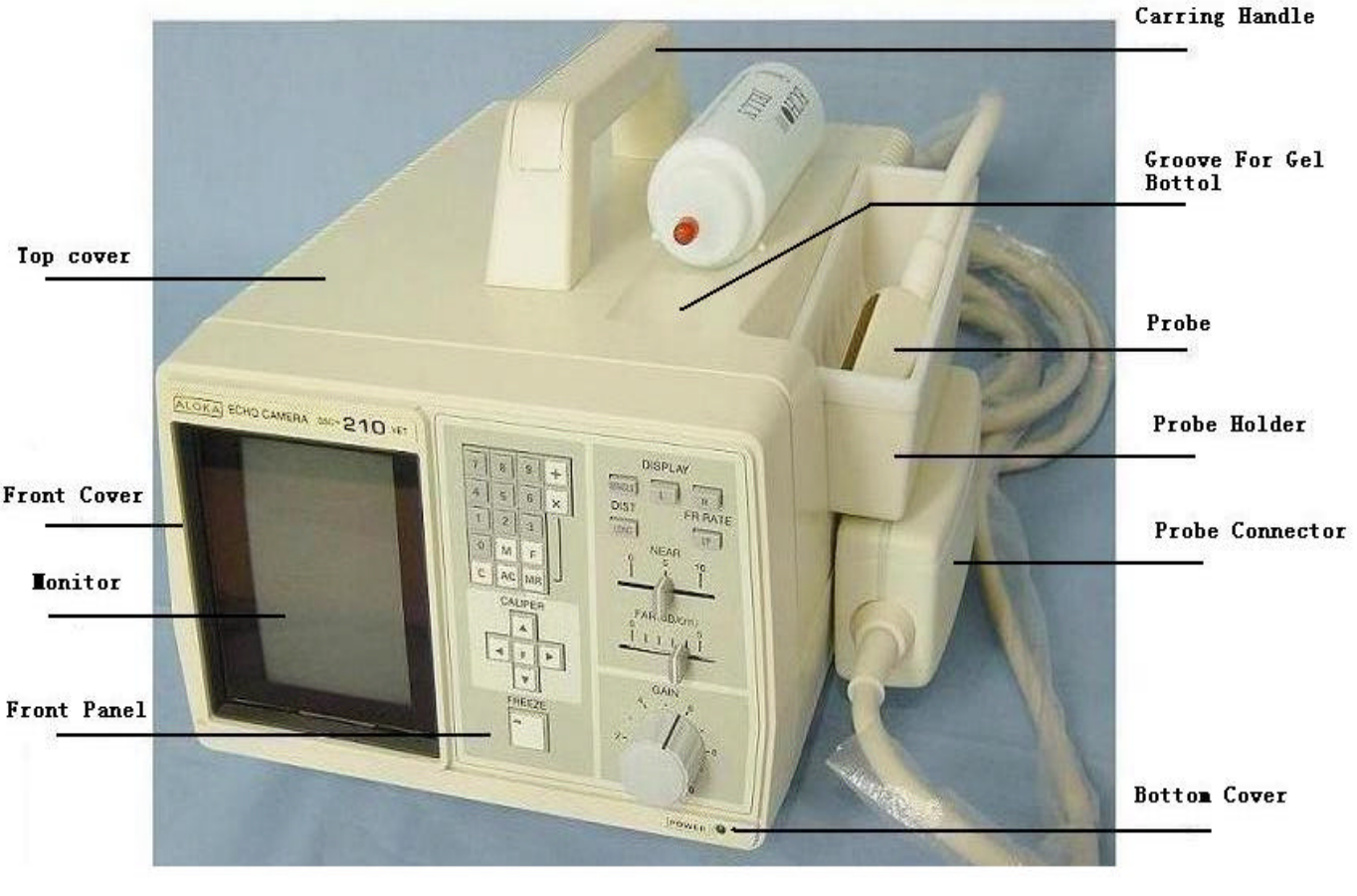
1-1 UNIT INDENTIFICATION

1-1. UNIT IDENTIFICATION



SECTION 1. PRINCIPLE OF OPERATION

1-2 SYSTEM PRINCIPLE

1-2 Basic Block Diagram

Basic block diagram and system block diagram are in Fig.1-2-1 and Fig.1-2-2 respectively
General operation of each block is described below.

1) Transmitter & Receiver

   This block provides the BURST wave by receiving the control signal transmitted from DSC. It generates the transmission trigger TRIG 1 to 8, based on this BURST wave RIG 1 to 8 are send to probe.. Received echo 1 to 8 sent from Probe are amplified under the control of GAIN and STC, and sent to DSC as ECHO VIDEO signal.

2) Probe

   The probe has eight blocks of circuits consisting of the transmitter amp, receiver preamp, 8-channal analogue multiplexer and counter. TRIG1 to 8 sent from Transmitter & Receiver is amplified by the transmitting amp. So as to generate the pulse for driving the transducer. The echo signal received by the transducer is amplified by the preamplifier and sent to Transmitter & Receiver Board. Analogue multiplexers are connected to 64 elements of transducers and perform the electronic scan by the control signal.

3) DSC

Ultrasound echo video signal sent from Transmitter & Receiver is converted to 4-bit digital data by A/D converter.

Converted video data of 8 pixels are stored and they are written in image Memory at the same time.

Memory address for writing are generated synchronizing with Ultrasound transmission timing.

On the other hand, Memory address for reading are generated synchronizing with TV-scanning signal.

Data of 8 pixels are also read out at the same time and using parallel-sirial conversion, Data of each pixel can be obtained

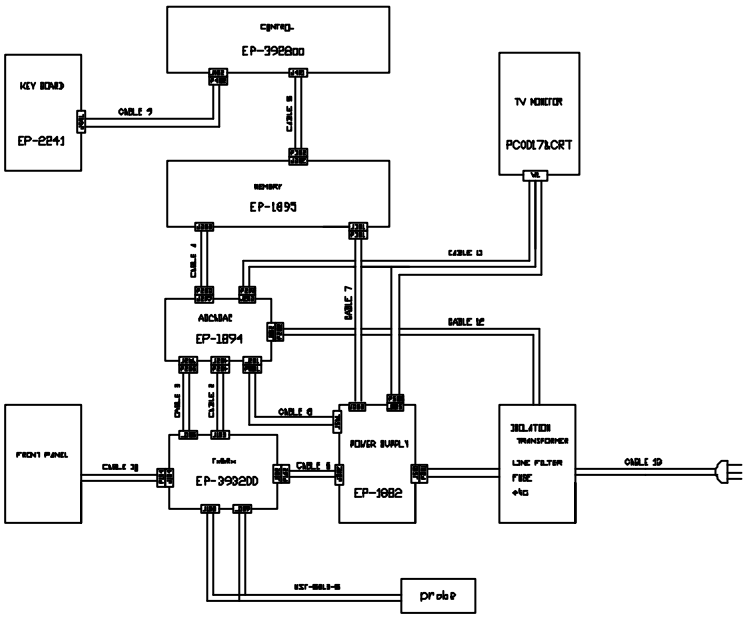
Two Line Memory are provided on MEMORY PCB, each Line Memory can store each video data of one Ultrasound scan line.

Post-process by line-to-line-interpolation is preformed by adding Data read out from Image Memory and Data read out from Line Memory.

Ultrasound image is smoothed by this processing method.

Digital ultrasonic data are added with graphic data read out Graphic Memory, gray-scale data and composite sync signal sent from Control PCB, and then sent to D/A converter to be Converted to analogue TV signal(composite video).

Such a series of operations are controlled by the control signal generated at Control PCB.



CONNECTOR DIAGRAM

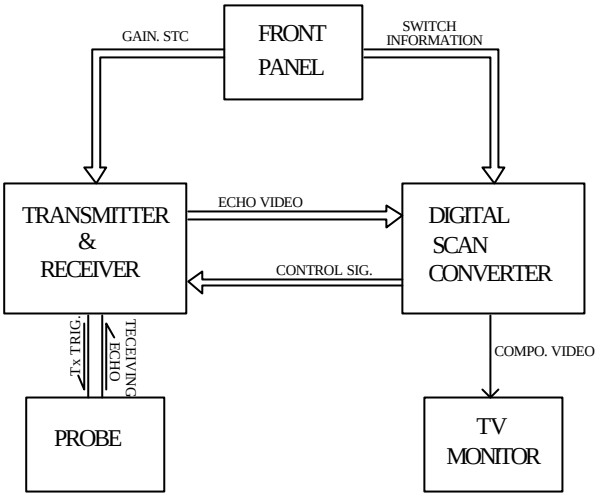


Fig. 1-2-1 SSC-210VET BASIC BLOCK DIAGRAM -1

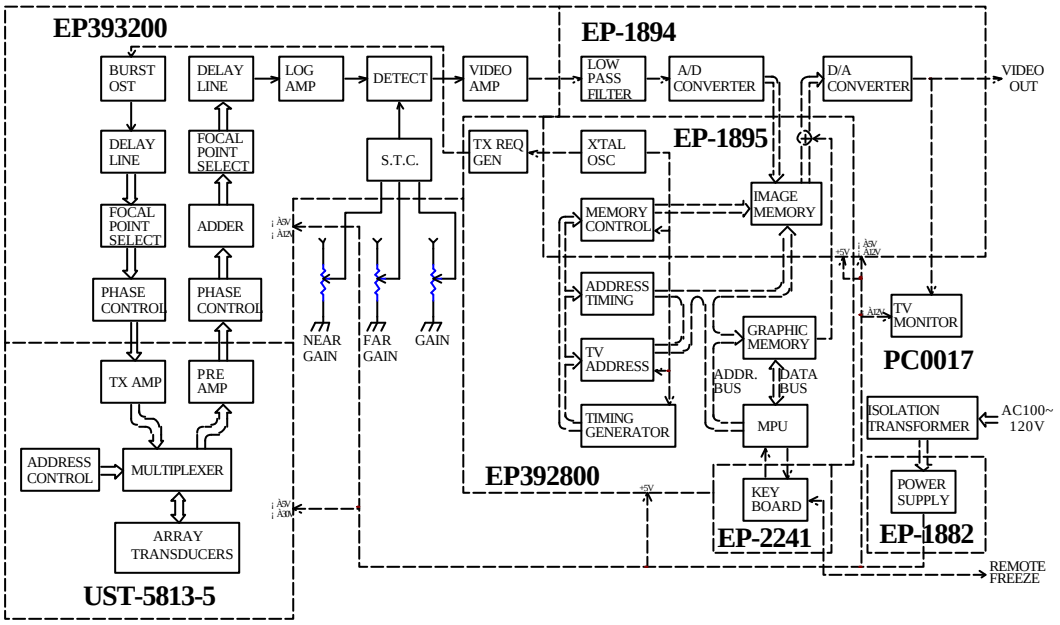


Fig. 1-2-2 SYSTEM BLOCK DIAGRAM

SECTION 1. PRINCIPLE OF OPERATION

1-3 PROBE UST-5813-5

1-3 PROBE UST-5813-5

Probe is composed of Array transducers, where 64 transducers are arranged linearly and two PC boards. Each PC board consists of four hybrid Ics having the functions of the transmitter amp, and receiver preamp, four 8-chanel analogue multiplexers and two 4 bit × 2 counters.

1) Scan Control

Signals CTRL 1 to 8 from Transmitter & Receiver board are used as clock inputs of 4-bit binary counter.

3 bits out of 4 bit counter output control SCAN ADDRESS as a decode signal of Analogue Multiplexer.

2) Transmission

Signals TRIG 1 to 8 from Transmitter & Receiver board are amplified by the transmitter amp and are supplied as the input of the Analogue Multiplexer. This multiplexer has 8 channels. One multiplexer makes selection of 8 transducers. One selected transducer is driven by receiving the signal from the transmitting amp. The same operation is performed in 8circuits. But when the focal point is near, 6 transducers are driven.

3) Reception

Echoes reflected in a living body are received by the selected 8 transducers and supplied to the input of the receiver preamplifier after passing through Mulltiplexer. Amplified echoes are sent to Transmitter & Receiver board via the probe cable.

SECTION 1. PRINCIPLE OF OPERATION

1-4 TX & RX UNIT EP393200

1-4 TX & RX UNIT EP393200

Transmitter and Receiver Board is composed of Transmitter which sends the transmission trigger to Probe by the control of DSC, and Receiver which sends the received echo to DSC after the control of GAIN and STC. Block diagram of Transmitter & Receiver Board is shown in Fig. 1-4-1.

1) Transmission

Pulse which oscillated in BURST oscillator circuit becomes pulse having delay of the specified by passing through the delay line. This delayed pulse is selected and send to Probe to drive the transducer, and ultrasonic beams are focus system, by the electronic focus system. In the electronic focus system, by sending beams from both sides of transducers in one block in order, ultrasonic beam is focused as if the block were arranged in concave.

In this system two focal points are available in depth direction. Either one can be selected by FR RATE switch on the front panel. 114 ultrasonic beams can be obtained by shifting the position of transducers one by one to shift the position of the position of the ultrasonic beam.

2) Reception

REC SIGNAL send from probe must be composed after phase-alignment because the distance between the echo source and each transducer is different. The phase is aligned by using Delay line. At this time, two beams(right and left), which shift to the right and left respectively by 1/2 pitch of the transducer against the beam center, are obtained.

Consider about FAR focus. the delay amount for the echo received by transducer NO.1 at Right and the delay amount for the echo received by NO.8 at Left must be the same. Delay amount for the echo received by transducer NO.1 at Left and delay value for the echo received by NO.1 at Right are the same. Similarly, 2 corresponds to 7, 3 to 6 and 4 to 6. Selection of Right and Left is controlled by the analogue switch. Signals whose phases have aligned by the above-described method are added and pass through LOG AMP, Detector circuit to set the maximum amplitude of the signal to 2v. Then, it is sent to DSC.

3) Generation of the BURST wave

Pulse for driving are oscillated by BURST oscillator circuit. The transmission position of the driving pulse is determined by TXRQ/signal supplied from DSC and the oscillation frequency depends on the frequency of Probe.

4) Address Control

When the FRAME RATE switch is set UP,4-bit signal CTRLA to CTRLD, are generated using TXRQ/ as clock input of the binary counter. CTRLA to CTRLD are used for phase control and CTRLA to CTRLC are also used as input code of Decoder. Decoder output CTRL1 to CTRL8 are sent to the binary counter for the address control of Probe. 3-bit output of the binary counter is used as the switch code of Multiplexer. When the RATE switch is set OFF, the above signal are generated based on NEAR/ instead of TXRQ1.

5) 8-channel Mutiplexer

Since 6 to 8 transducers are used in one block, the distance between the echo source and each transducer is different. Thus, the phase of echo signal must be aligned. 8-channel Multiplexer is used for phase alignment.

6) Log Amp.

Received echoes after phase aligned and added are log-compressed by Log Amp circuit. Signals amplified or attenuated by +60db, +30db,0db, and –30db by High Frequency amp., Buffer and Attenuator are log-added by Log Ic to obtain Log output with dynamic range of 120db. Log output are taken out from two output terminals(phase is different by π(rad)). Each signal is amplified and sent to Detector circuit with the amplitude uniform.

7) STC

STC SIG. is generated by STC SIG Generator and sent to Detector. The sound pressure of the reflected echo from a living body depends on diagnostic depth and other conditions. Therefore, in order to obtain the best diagnostic image at each time, set the amplitude of the received echo to the optimum level by adjusting GAIN, NEAT and FAR in the front panel.

8) Detector

Information of the received echo can be obtained as an envelope of the received signal. The output signal of Log amp is detected by Detector circuit and sent to Video circuit.

9) Video Amp

Video Amp circuit amplifies the signal to obtain the output voltage required for input to TV monitor. Also, by zero Level Hold circuit, the video amp output is always kept to 0v standard.

10) Explanation of each timing signal

USBLK Used as the basic signal for generating STC SIGNAL. Also this is used as the control signal of zero level hold circuit for the video signal. CTRLA to C Used as 3-bit input code of 8-channel Multiplexer which is used for phase alignment of the reception/transmission signal. This is also used as the input code of Decode generating CTRL1 to 8 which is sent to Probe. CTRLD Used as the signal for selecting Right or Left in Micro-Angel sector method which is performed in reception. T1 to T4 These are source of "TRIGx" which are sent to Probe, and obtained by delaying the signal oscillated by BURST oscillator by the specified amount. Delay amount is $T1 \leq T2 \leq T3 \leq T4$. TRIG 1 to 8 Signals obtained by such a way where T1~4 signals pass through Matrix circuit, composed of eight 8-channel multiplexers, and are controlled by CTRLA~C.

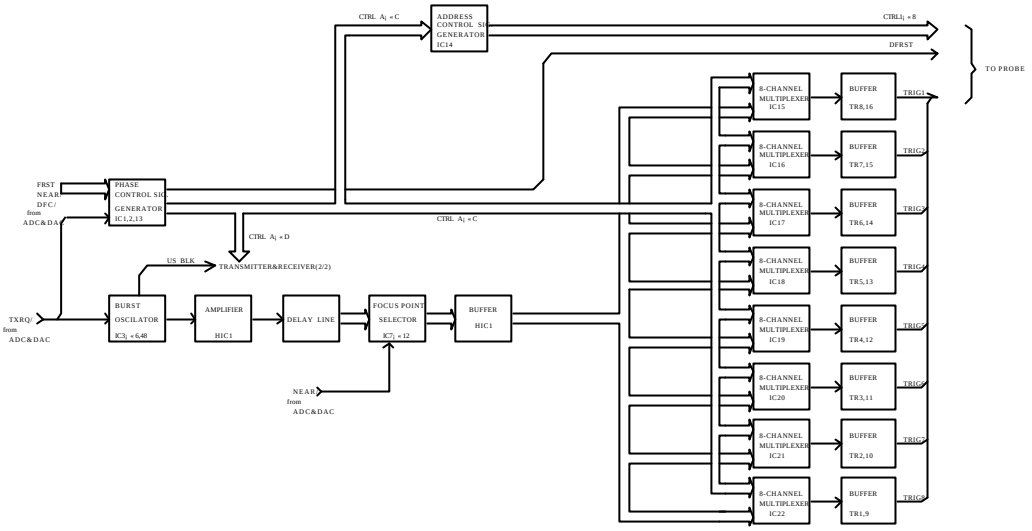


Fig. 1-4-1 TRANSMITTER & RECEIVER BLOCK DIAGRAM

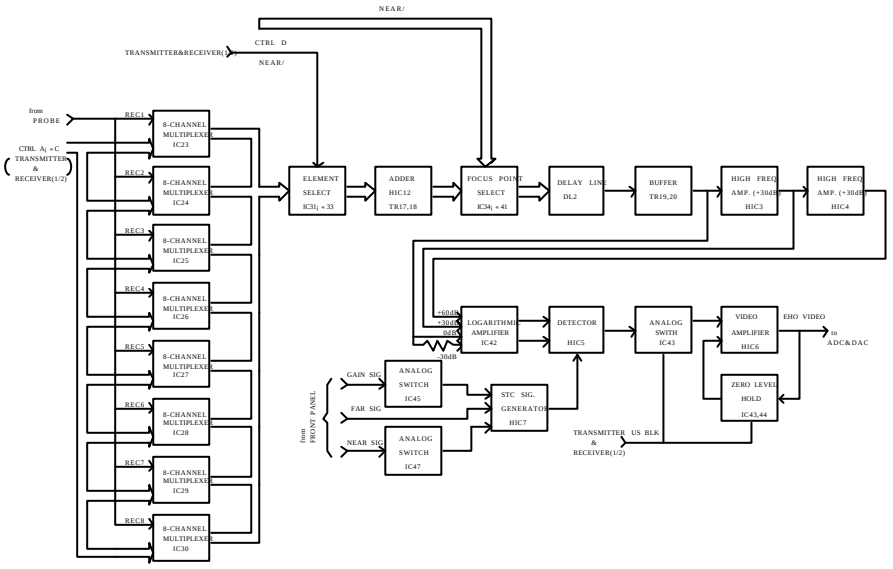


Fig. 1-4-1 TRANSMITTER & RECEIVER BLOCK DIAGRAM (2/2)

SECTION 1. PRINCIPLE OF OPERATION

1-5 D.S.C. UNIT

1-5. DSC

1-3-1. GENERAL

1) This DSC unit is exclusive for linear-scan method designed for handy-type electronic linear scan diagnostic equipment.

2) This DSC unit is composed of three PC boards and one switchboard Power Consumption is approx. 10w.

3) Image Memory has memory capacity of 480*256*4 bits, and Graphic Memory For caliper and ID indication has a capacity of 256*256*1 bits. Information of two memories are displayed on TV screen as a composed image.

4) DSC unit controls the transmission timing of the ultrasonic wave and Transmission position. Transmission stops in the picture freezing condition.

5) For the change of number of scanning lines, that is change between 525 lines/60Hz and 625 lines/60Hz,a crystal and 2 ROM Ics must be replaced.(A Crystal is soldered. Rom is equipped on an IC socket.)

1-5-2 Composition

1) DSC module is composed of three PC boards for circuits (280*140mm) and PC board for switches (131*44mm), and the following voltage and capacitance are required as a desired power source.

DSC block diagram is shown in Fig.1-5-1

PC unit

EP-1894 ADC, DAC (280*150*10mm) 1 piece
EP-1895 Memory (280*150*10mm) 1 piece
EP-392800 Control (280*150*10mm) 1 piece
EP-2241 Key Board (131*44*15mm) 1 piece

Required power source

DC + 5V	±5%	Approx. 1.5A
DC – 5V	±5%	Approx. 70mA
DC+12V	±20%	Approx. 50mA

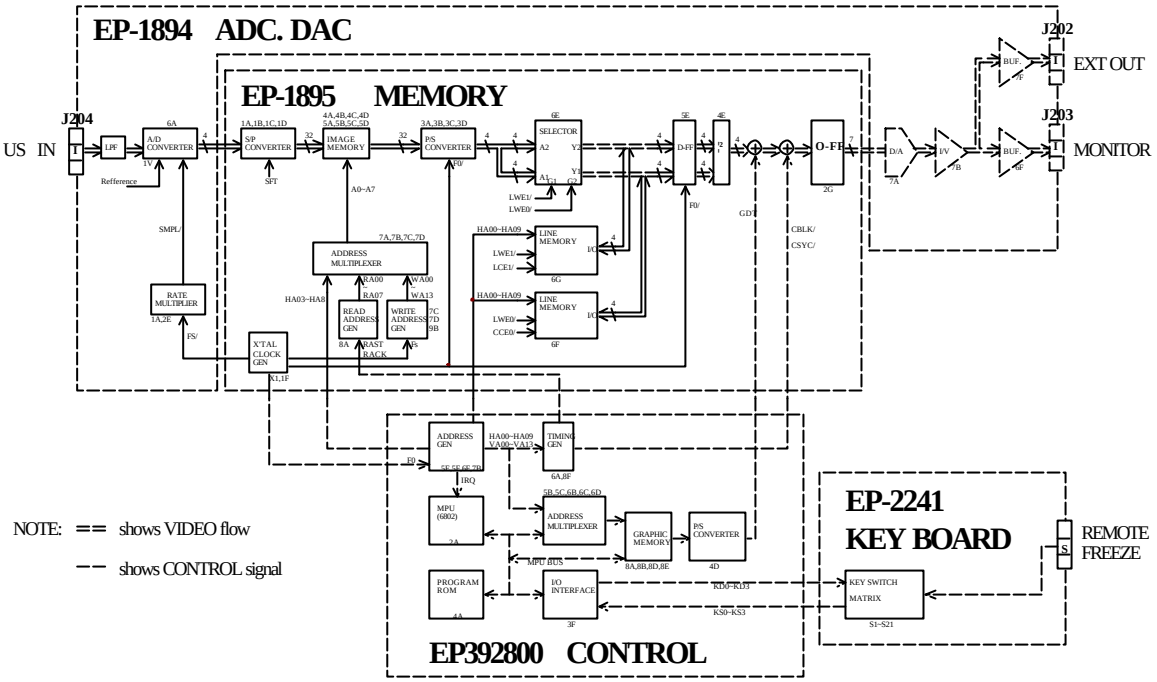


Fig. 1-5-1 DSC BLOCK DIAGRAM

SIGNAL	FULL NAME OF SIGNAL	EXPRANATION OF ACTION OF SIGNAL	SOURCE AND ROUTE OF SIGNAL
A0-A7	Address	Multiplexed image memory address	MEMORY
AD0-AD3	A/D Data	A/D Converter output	MEMORY
AR00-AR13	Address	MPU Address	CONTROL
CAS	Column address strobe	D. Ram CAS signal	CONTROL→MEMORY
CBLK	Composite blank	TV Blanking signal	CONTROL→MEMORY
CHG0-CHG5	Change	Focus exchange data	ADC.DAC→MEMORY
COL	Column address	D.Ram column address select	MEMORY
CSYC	Composite sync	TV Synchronous signal	CONTROL→ADC.DAC
D0-D7	Data	MPU Data	CONTROL
DA1-DA7	D/A Data	D/A Converter input	AD.DAC
DFC	Focus	Focus control	ADC.DAC→Tx&Rx
DFON	Focus on	Focus control	CONTROL→MEMORY
DYNF	Focus	Focus control	MEMORY→ADC.DAC
E	Enable	MPU Enable signal	CONTROL
ET	Enable T	Rate multiplier output	ADC.DAC→MEMORY
EXT.OUT	External output	TV signal output 2Vp -p at open Zo=75 ohm	ADC.DAC
Fo,Fs	System clock	Fo=Fs,525Lines=10.08MHz 625Lines=10.08MHz	ADC.DAC→CONTROL →MEMORY
FRST	Frame reset	US Frame synchronous signal	ADC.DAC→Tx&Rx
FSTT	Frame reset	US Frame synchronous signal	MEMORY→ADC.DAC
FSYC	Frame reset	US Frame synchronous signal	MEMORY→CONTROL
FULL	Full pixel	Select 480 pixels or 416 pixels	CONTROL
FZRQ	Freeze request	Freeze control	CONTROL→MEMORY

SIGNAL	FULL NAME OF SIGNAL	EXPRANATION OF ACTION OF SIGNAL	SOURCE AND ROUTE OF SIGNAL
GA00-GA12	Graphic memory address	Select graphic memory address	CONTROL
GD0-GD7	Graphic data	Parallel graphic data	CONTROL
GDT	Graphic data	Serial graphic data	CONTROL→MEMORY
GMA	Graphic memory address select	TV address select signal	CONTROL
GRAM	Graphic memory select	Graphic memory select by MPU	CONTROL
GREN	Graphic enable	Graphic display enable	CONTROL
GSFT	Graphic sift clock	P/S Converter sift clock	CONTROL
GWT	Graphic write timing	Graphic write timing for MPU	CONTROL
GY0-GY3	Gray scale data	Gray scale data,16levels	MEMORY
GYEN	Gray scale enable	Gray scale display enable	CONTROL→MEMORY
HA00-HA09	Horizontal address	TV Horizontal direction address	CONTROL→MEMORY
HRST	Horizontal reset	TV Horizontal address reset	CONTROL
HSL0-HLS3	Horizontal select	Horizontal line type select	CONTROL
IMEN	Image enable	US Image display enable	CONTROL→MEMORY
INH	Inhibit	Graphic memory access inhibit by MPU	CONTROL
IO	Input,Output	I/O interface select signal	CONTROL
KD0-KD3	Key switch drive	Key board matrix drive	CONTROL→KEY BOARD
KS0-KS7	Key switch sense	Key board matrix sense	CONTROL←KEY BOARD
LCE0-LCE1	Line memory chip enable	Line memory chip enable	MEMORY
LCNT	Level control	Video level control	MEMORY
LD0-LD7	Line data	Line memory data	MEMORY
LMEN	Line memory enable	Line memory access enable	CONTROL→MEMORY
LMP	Lamp	Freeze lamp drive	CONTROL→KEY BOARD
LOWC	Low contrast	Contrast level control	NOT USED
LTV	Latch video data	S/P Converted data latch clock	MEMORY
LWE0-LWE1	Line memory write enable	Line memory write enable	MEMORY

NOTE: In the circuit diagram,"/" indicates "Low" active of signal polarity.

D.S.C SIGNAL EXPRANATION

SIGNAL	FULL NAME OF SIGNAL	EXPRANATION OF ACTION OF SIGNAL	SOURCE AND ROUTE OF SIGNAL
MAG	Magnify	US Image display size select	CONTROL→ADC.DAC
MD00-MD31	Memory data	Image memory data, 8 pixel in parallel	MEMORY
MON1.OUT	Monitor out	TV Signal for internal TV monitor	ADC.DAC
MPCK	MPU Clock	MPU Clock,Fo/16	CONTROL
MSEL0-MSEL3	Memory select	Graphic memory chip select	CONTROL
NEAR	Near focus operation	Near focus state	ADC.DAC→Tx&Rx
NERF	Near focus state	Near focus state	MEMORY→ADC.DAC
00-07	Output	Output data from sampling ROM	ADC.DAC
PED	Pedestal	TV Pedestal	CONTROL→MEMORY
R/W	Read/Write	MPU R/W Signal	CONTROL
RA00-RA07	Read address	Image memory read address	MEMORY
RACK	Read address clock	Read address counter clock	CONTROL→MEMORY
RACKE	Read address clock enable	Read address counter clock enable	CONTROL
RAME	RAM enable	Graphic memory enable	CONTROL
RAS	Row address strobe	D.RAM RAS Signal	CONTROL→MEMORY
RAST	Read address set	Read address counter reset signal	CONTROL→MEMORY
RASTE	Read address set enable	Read address counter reset enable	CONTROL
RCHG	Read exchange	Read focus exchange data	CONTROL→MEMORY ADC.DAC
READ	READ	Grahpic memory read signal	CONTROL
SD0-SD3	Serial data	P/S Converter output signal	MEMORY
SF0-SF1	Spare function	Spare signal	KEY BOARD
SFT	Shift	S/P converter clock	MEMORY
SMPL	Sample	A/D Converter clock	ADC.DAC
SYC	Synchronous	MPU clock synchronous signal	CONTROL

D.S.C SIGNAL EXPRANATION

SIGNAL	FULL NAME OF SIGNAL	EXPRANATION OF ACTION OF SIGNAL	SOURCE AND ROUT OF SIGNAL
TRST	Timing reset	Memory basic timing reset signal	CONTROL→MEMORY
TSYC	Tx synchronous	Tx Timing signal	CONTROL→MEMORY →ADC.DAC
Tx REQ	Tx Request	Tx Timing signal	ADC.DAC→Tx&Rx
TXRT0-TXRT1	Tx Rate	Tx Rate select	NOT USED
USIN	US Image input	Analog video signal input from Rx	Tx&Rx→ADC.DAC
VA00-VA09	Vertical address	TV Vertical direction address	MEMORY
VD0-VD3	Video data	Serial video data	ADC.DAC→MEMORY
VMA	Valid memory address	MPU VMA signal	CONTROL
VRST	Vertical reset	TV Vertical counter reset signal	CONTROL
WA00-WA13	Write address	Image memory write address	MEMORY
WE	Write enable	D.RAM we Signal	CONTROL→MEMORY
WEN	Write enable	Image memory Read/Write select	MEMORY
WRT	Write state	Image memory write address select	MEMORY
WSTO	Write strobe	DSC Control register write strobe	CONTROL
625	625 Lines	625 Lines/50Hz TV System	

1-5-3 Operation

1) EP-1894 ADC,DAC

a) A/D conversion

Video signal from Transmitter/Receiver is input to the “US IN” terminal and fed into the analog input terminal of A/D converter IC6A after passing through the low-pass filter (fc=2.5MHz).Since the loss of the low-pass filter is approx.6dB,though the signal level at the input side is 0 to 2V,that at the output side is 0 to 1V.

Since the REF voltage of A/D converter is set to 1V and four bits are the conversation bits, the output of “0000” is obtained when the signal of 0V is input to “US IN”, and the output of “1111” is obtained in case of +2V input.

The clock of A/D converter is fixed to 1/2FS.A/D converted video data are latched in IC2F once and then sent to S/P converter in Memory Unit.

b) D/A conversion

Digital video signal read out from Image Memory is fed to the input terminal of D/A converter IC7A to be converted to the analog signal.

Since the output of D/A converter is current –output ,the current-to-voltage conversion is performed by Ope amp IC7B to obtain 2vp-p composite video signal. This output passes through Buffer IC7F, and becomes the external output “EXT OUT”. On the other hand, this output is divided by 2 and sent to CRT through the analog switch IC7D and Buffer IC6F.

c) Rate Multiplier

8-bit rate multiplier is used to decide the sampling rate corresponding to each probe and diagnostic distance. The constant corresponding to each diagnostic distance is read out from ROM 2E, and added by the system clock “FS”. When the added result is over 255, its carry signal is generated to be sampling clock of data. Though A/D conversion is performed at a constant interval (1/2 FS),writing in Image Memory is performed at the timing of carry signal. Also, changing point information at the dynamic focus and transmission time interval corresponding to each diagnostic depth are sent out from ROM 2E,and supplied to each control circuit

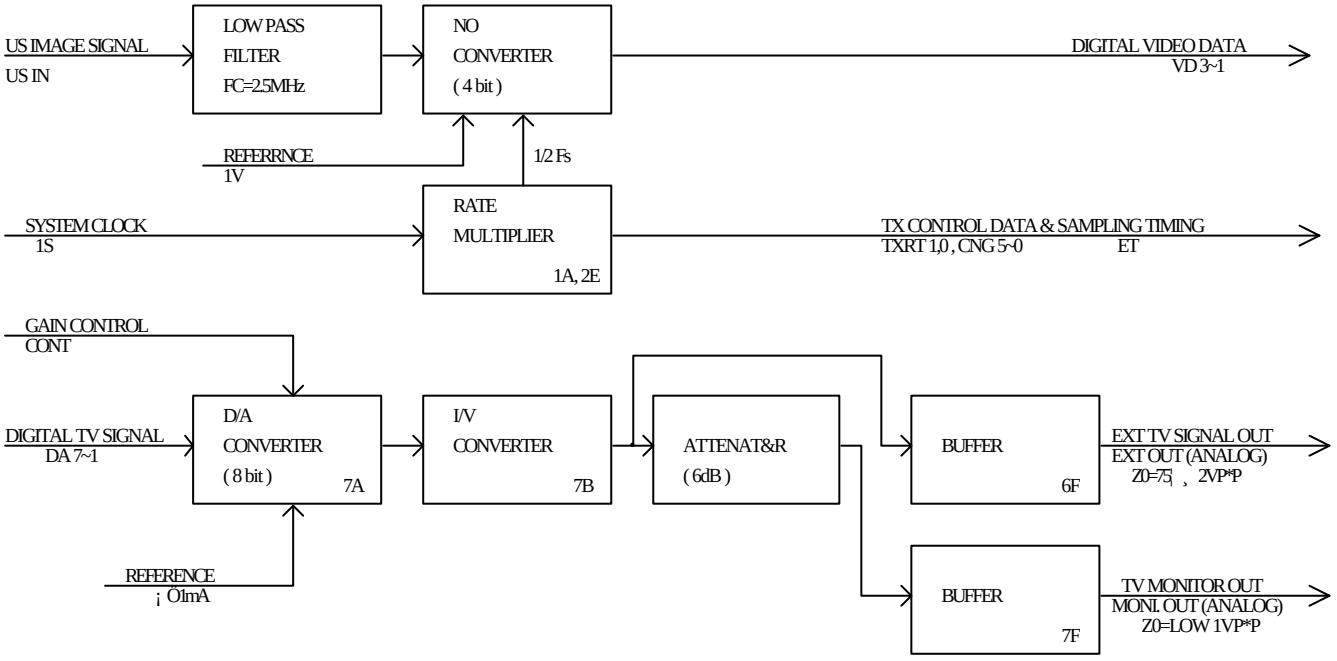


Fig. 1-5-2 ADC DAC BLOCK DIAGRAM

2) EP-1895 Memory

a) Image Memory

Image Memory is composed of S/P converters, Memory and P/S Converters. S/P converters and P/S Converters are not required fundamentally. But since the operation speed of Memory is slower than the input/output speed of data, these circuits work as interface to write and read out 8-pixel data collectively.

A/D converted data are taken in Shift Register IC1A to 1D in S/P converters by the clock "SFT" synchronizing with the sampling clock.

When 8-pixel data are taken into Shift Register, they are latched in IC2A to 2D for written into Memory. 8-pixel data latched at the time except the time for reading for the TV indication are written in Memory.

Reading out for the TV display, 8 pixel that are same as the number of pixel at writing in are read out and loaded in Shift Register IC3A to 3D in P/S Converters. Loaded data are shifted out one pixel by one pixel by the system clock "F0" and pass through Buffer IC. Then in Correlation circuit, IC4E,5E,6F and 6G, the average of the addition with the data of previous line is obtained, and is added with the TV timing signal, gray-scale data and graphic data, then sent to D/A converter.

b) Image Memory Address

Memory addresses for writing and reading are required independently. Write address is generated by IC8B, 7C, 7D and 9B. Read address is generated by IC8A. Write address is counted up by the output of Rate Multiplier "ET". IC8A performs control at every 8 pixels, IC7C and 7D generate the address in the depth direction and IC9B generates the memory address in the lateral direction.

The first-order bit of IC9B is sent to transmitter/receiver as the synchronous signal of 1 frame of ultrasound image. Also, the address in the depth direction is compared with the information of focus change point sent from Rate Multiplier unit and performs the changing point control at the dynamic focus.

Since read address is synchronous with the TV signal, only address in the lateral direction is generated by IC8A and for the address in the depth direction, TV timing addresses HA08 to HA03 are used in common

Write address and read address are selected by Muliplexer IC6C, 6D, 7A and 7B and required one is supplied to Memory.

c) Gray Scale

Gray Scale Generator is composed of 2 stages of 4-bit counter IC5F and 5G, and generates 16-level gray scale signal at a rate of 30 pixels/level.

4-bit (16 levels) gray scale data are sent to D/A converter together with the image data.

d) System Clock

The system clock which is the basic clock of the whole DSC “FS, F0” is generated by a Crystal and logical gate IC 1F.

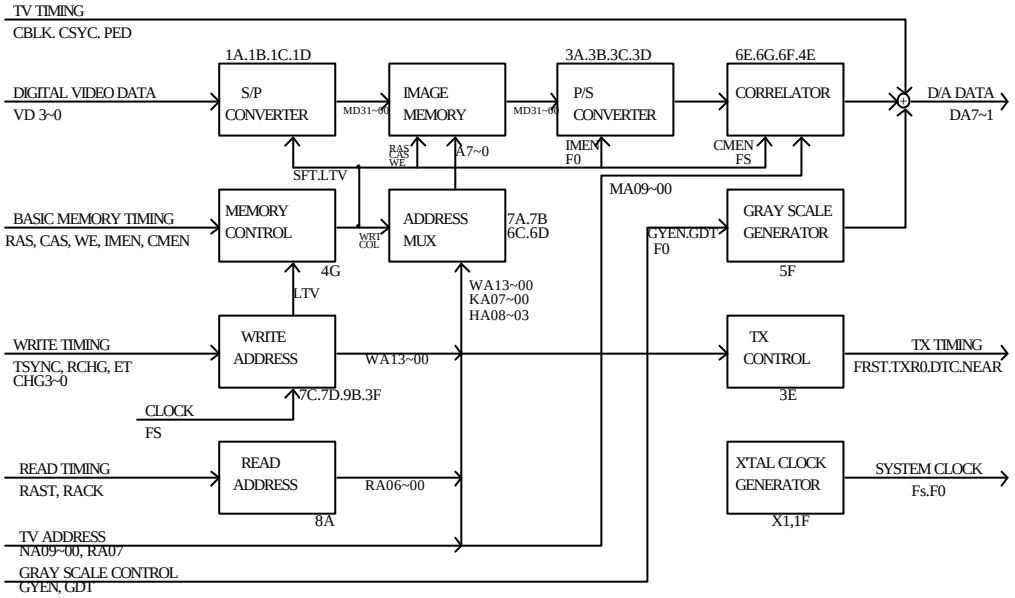


Fig. 1-5-3 MEMORY BLOCK DIAGRAM

3) EP-392800 CONTROL

a) Memory Timing

Basic timing required for the operation of the image memory is obtained by IC5E, 7E and 6E. The system clock F5 is divided by 16 by IC5E to obtain the address of Timing ROM 7E.

Data for timing signals required for the operation of Image Memory, RAS, CAS, WE, etc. are programmed in ROM. Data read out with a period of F0 are latched by IC6E and sent to Memory Control and other units.

b) TV timing

Blanking signal and synchronous signal which compose TV signal are generated by IC6F, 5F, 7B, 7C, 8F, 7F, 6A and 7A. Also the timing signal for reading out data from Image Memory is generated. System clock F0 is divided by 640 by IC5E, 6F and 5F to generate the address in the horizontal direction of TV scan and this generated address is supplied to Timing ROM 8F.

Horizontal blank, horizontal synchronous signal and memory timings required for TV signal are programmed in ROM. Data read out with a period of F0×1/8 are latched by IC7F and supplied to each circuit.
IC7B and 7C divide 1H of TV by 525 or 625 to generate the TV address in the vertical direction, and generated address is supplied to ROM 6A. Vertical blank, vertical synchronous signal and control signal for memory read address are programmed in ROM. Data read out at every 1H are latched by IC7A and supplied to each circuit.

Address in the horizontal direction and vertical direction are also used as the address of Graphic Memory.

c) Graphic Memory

Graphic Memory is an overlay memory to display caliper mark and ID information on TV screen. Since Graphic Memory is accessed by both TV read and MPU, Address Multiplexer IC6D, 6C, 6B and 5C selects the address.

In case of TV read, TV H and V addresses are select. Graphic data read out from Graphic Memory IC8E, 8D ,8B and 8A are loaded in IC4D for P/S conversation, and after shifted out with a clock period of 1/2F0 they are sent to D/A converter.

When MPU accesses Graphic Memory, address multiplexer selects the MPU address “AR”, and data line “D7 to D0” is connected to the data line of Memory by IC3D to make reading and writing possible.

d) DSC Control

All of condition controls of DSC are performed by internal MPC, IC2A. The program for MPU is stored in EP-ROM, IC4A and the capacity is approx . 4k byte.

The control input of DSC (switch information, etc.) is input to MPU via IC3F. Control information (freeze control, picture selection, focus selection etc.) out of the processed results are latched in IC3E and supplied to each part.

The information to be displayed graphically (ID code, mark etc.) are displayed on

TV screen by writing in Graphic Memory in bit-image.

The transmission time interval corresponding to each probe and diagnostic depth (transmission repetition cycle) is determined by IC2C, 2B and 1B and the timing signal “TSYC” is generated.

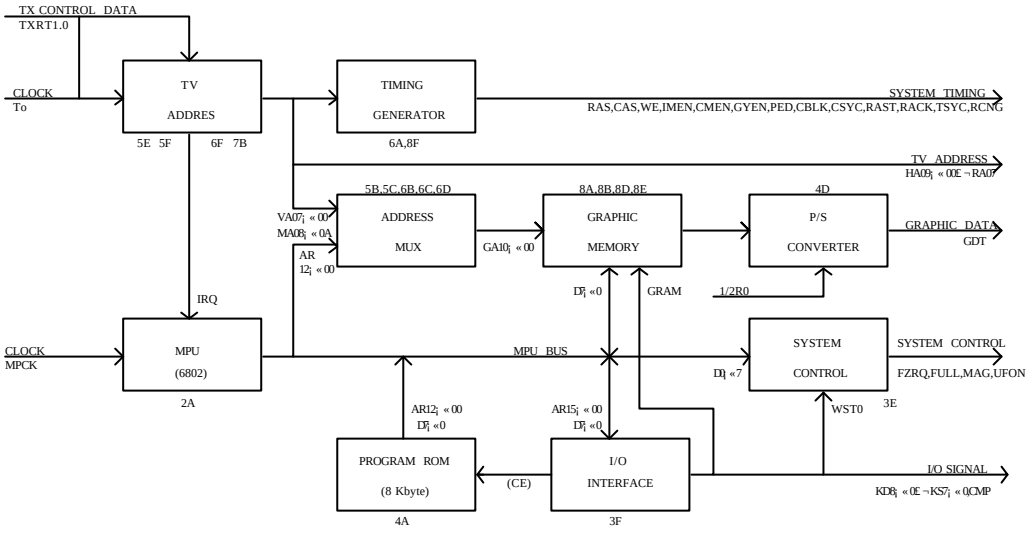


Fig. 1-5-4 CONTROL BLOCK DIAGRAM

4) EP-2241 KEY BOARD

This is the switch circuit where key switch for controlling DSC is placed at the intersecting point of “KD” and “KS” lines.

S21 (freeze switch) with LED is used for the indication of ON-OFF condition of freeze. At freezing, this LED lights up. Since the switch employs rubber-contract, the contact resistance is higher by several hundreds ohms.

4 switch input terminals from the external equipment (for DIST, FR RATE etc.), “4~1” and a common terminal to the switch “C” are provided.

Since all of switch information are taken in MPU, performance of operation depending on the switch condition is controlled by the program of MPU.
“ S21 (Freeze Switch) and K1 (Relay for remote freeze control) are assemble in parallel.

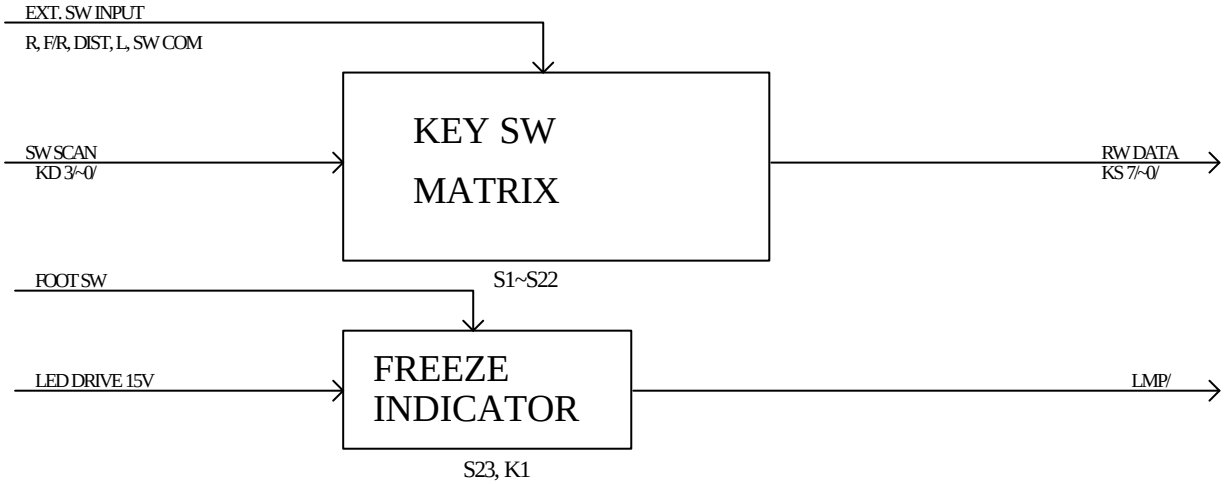


Fig. 1-5-5 KEY BOARD BLOCK DIAGRAM

SECTION 1. PRINCIPLE OF OPERATION

1-6 MONITOR IP-0503-TV

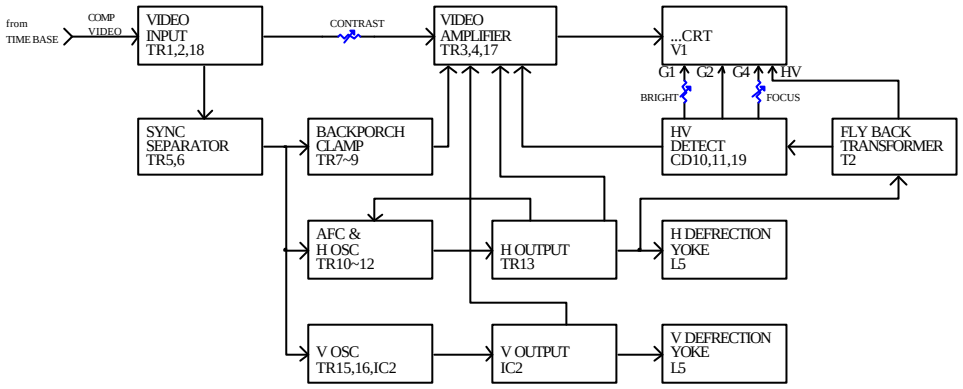
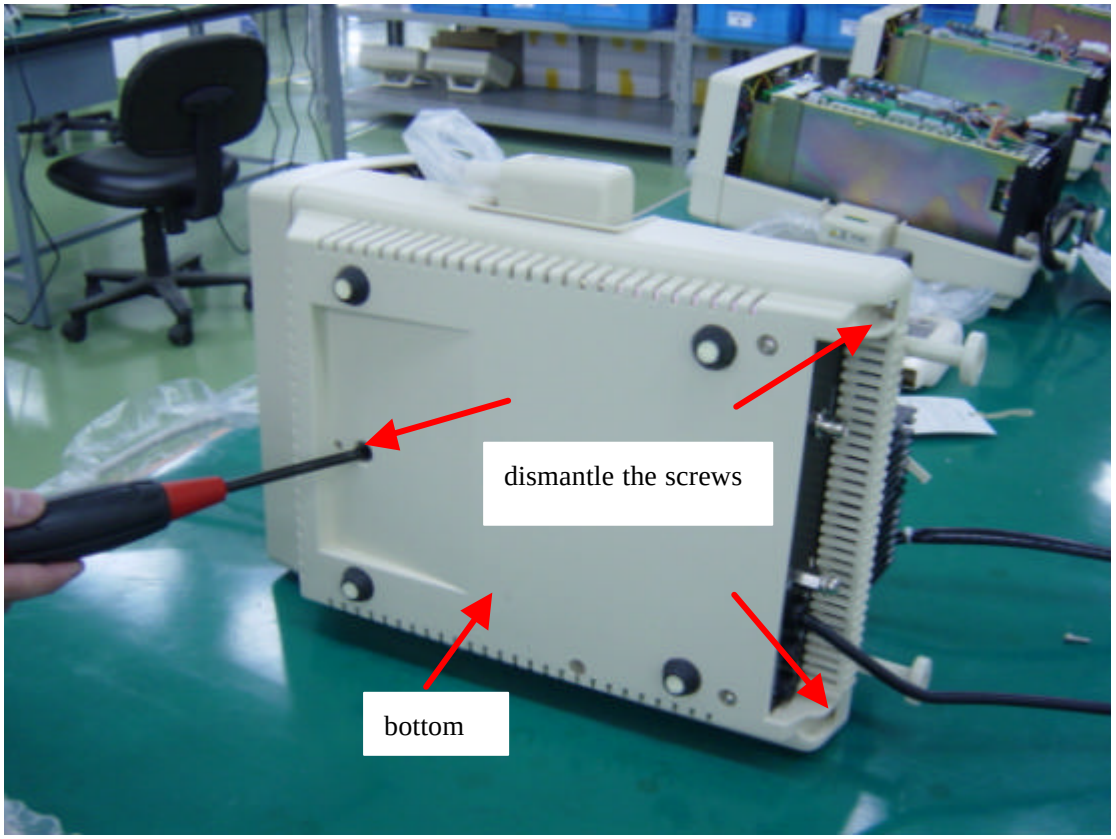


Fig. 1-5-6 TV MONITOR BLOCK DIAGRAM

SECTION 2. MAINTENANCE AND TROUBLESHOOTING

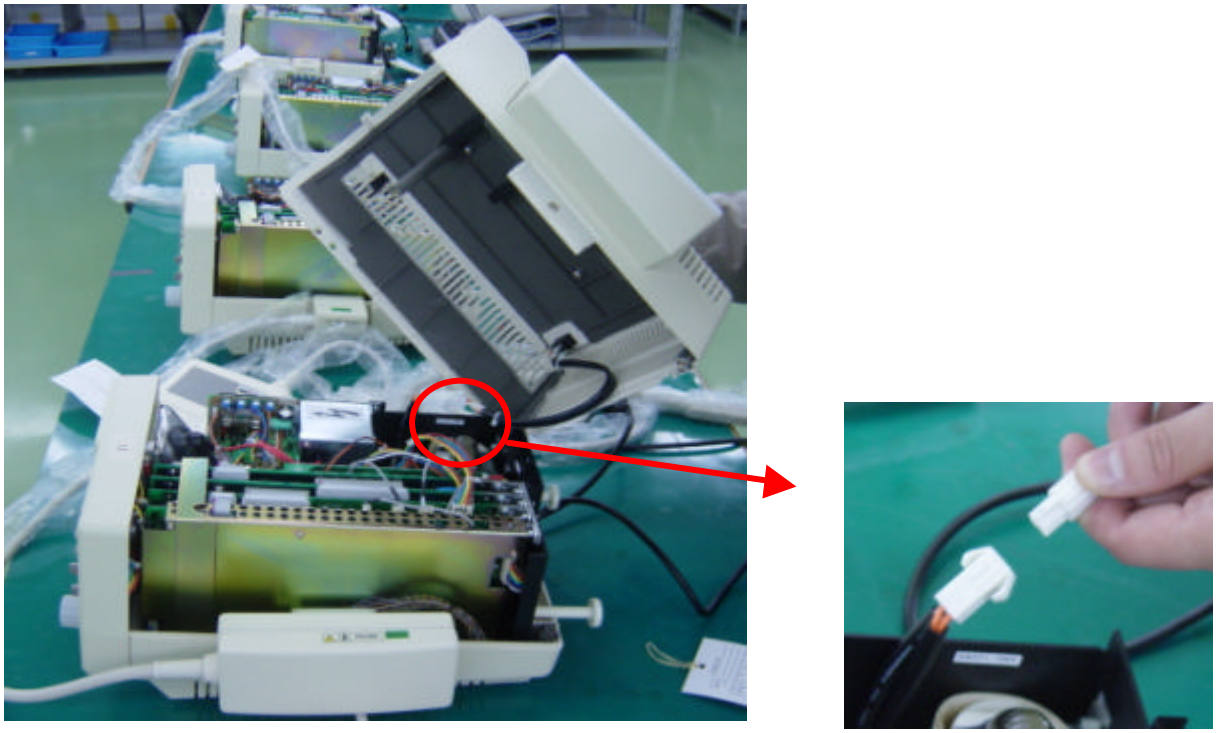
2-1. DISASSEMBING MANUAL

1. tilt machine to one side, dismantle three fixed screws of the bottom.

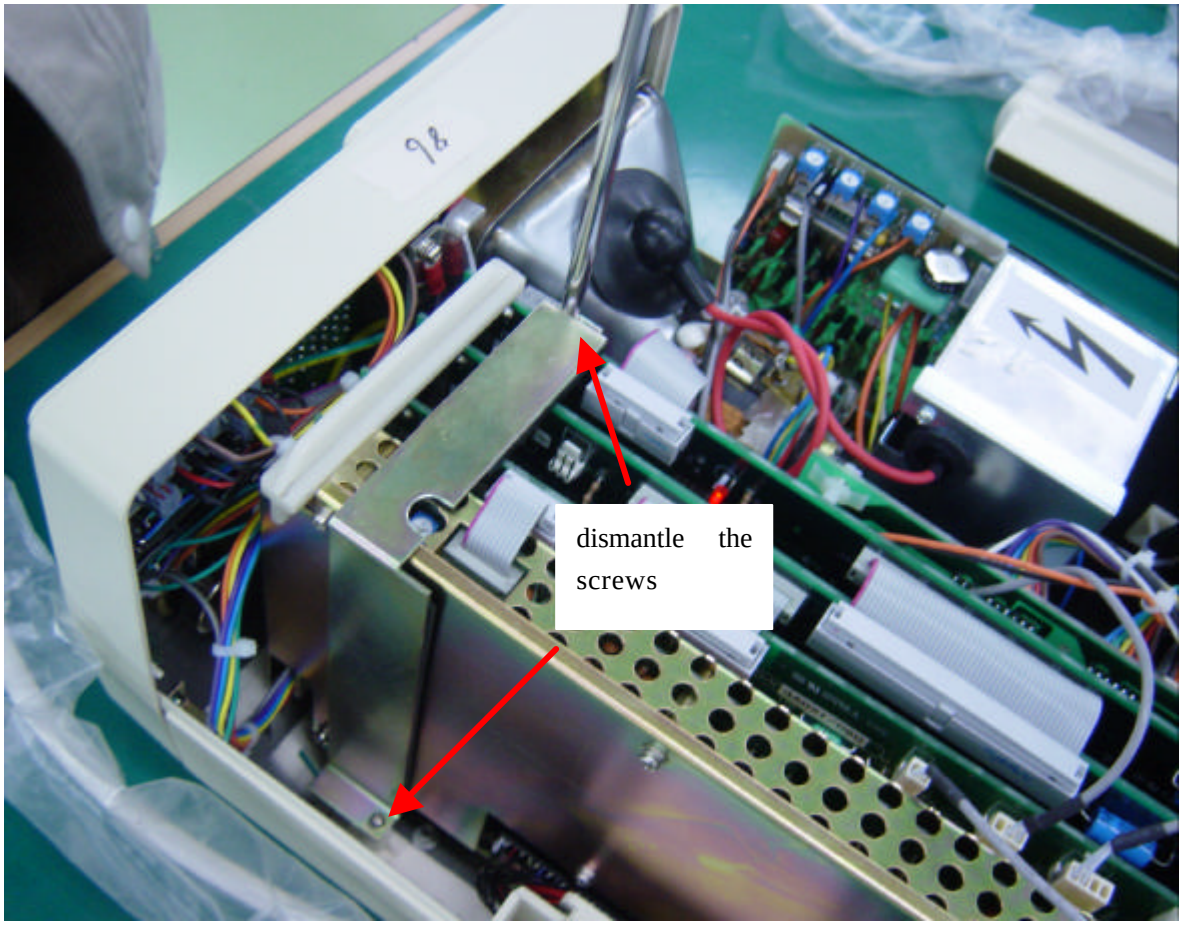


2. open machine's upper cover.

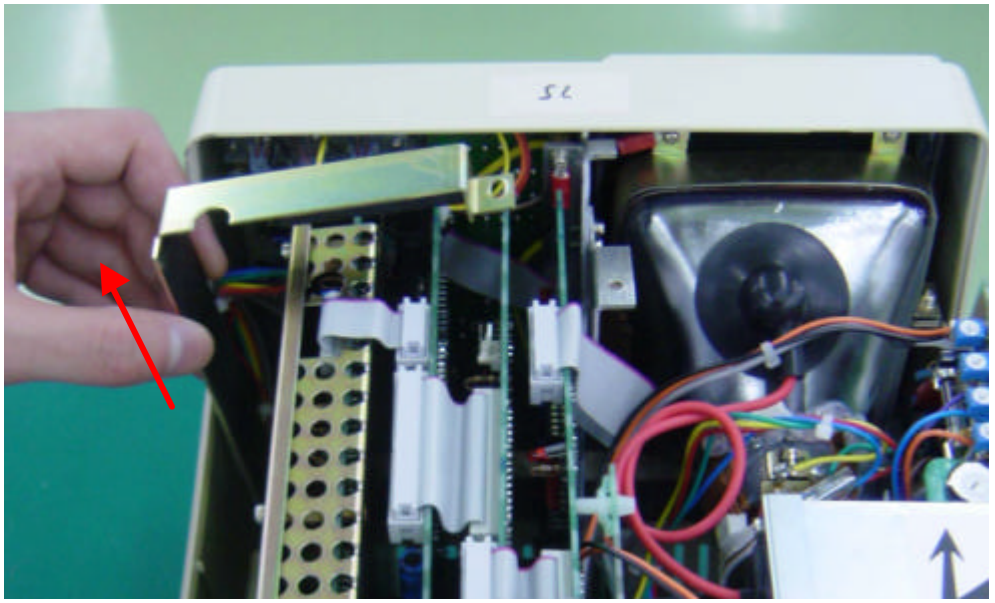
3. utile the connector



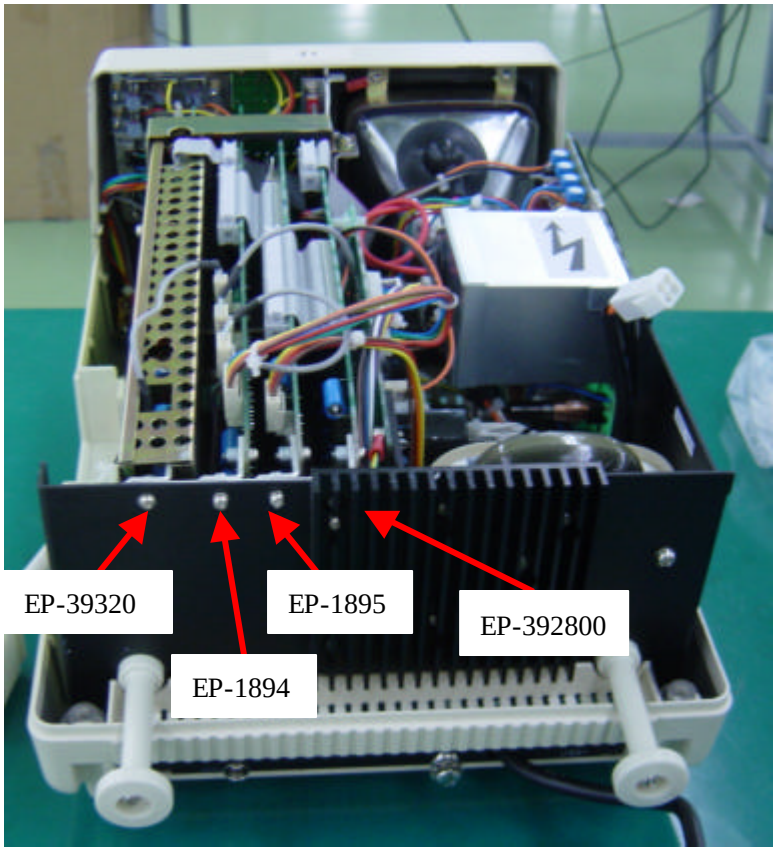
4. dismantle two screws and then open the plate which to fix pc board.



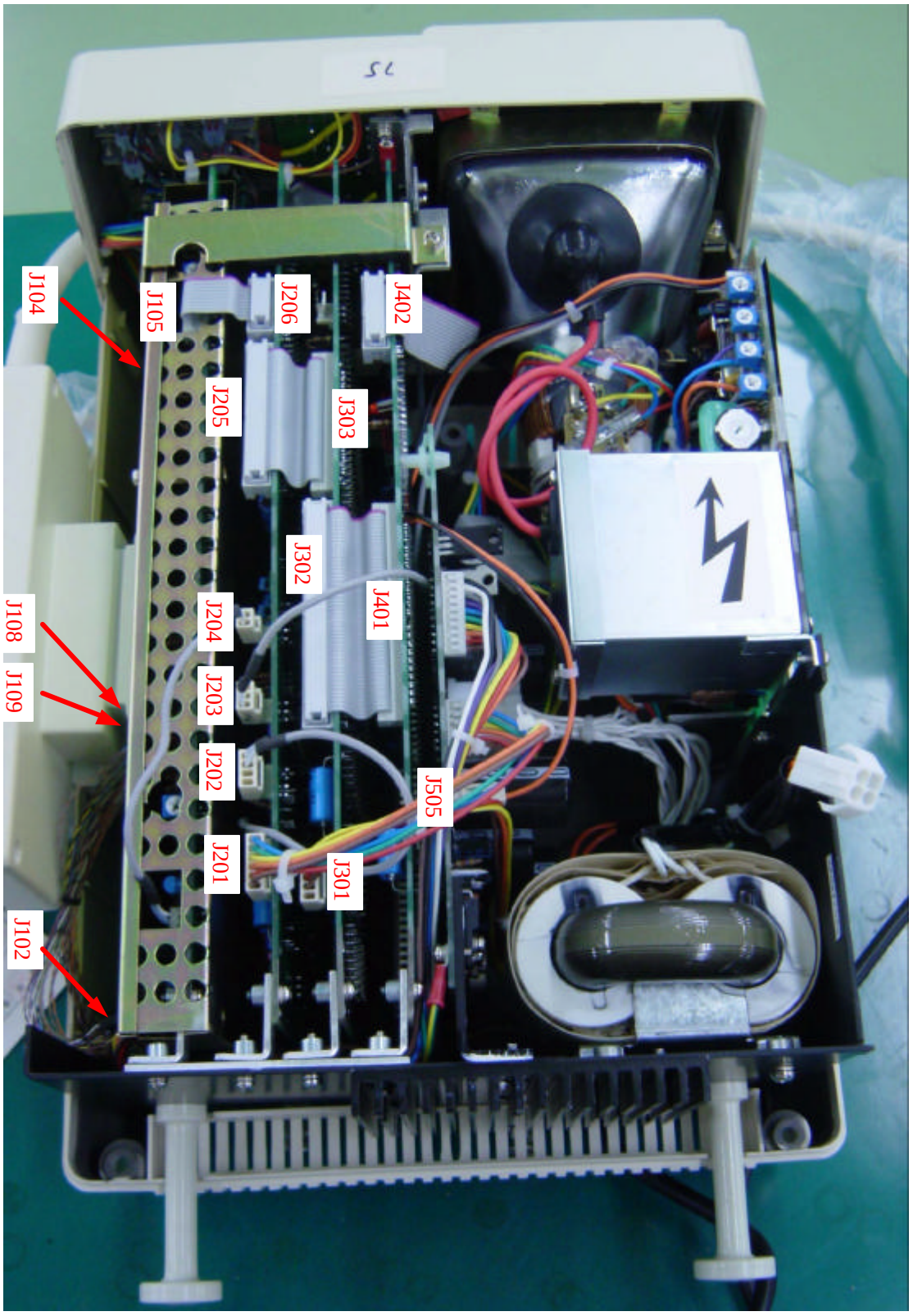
5. remove the plate.



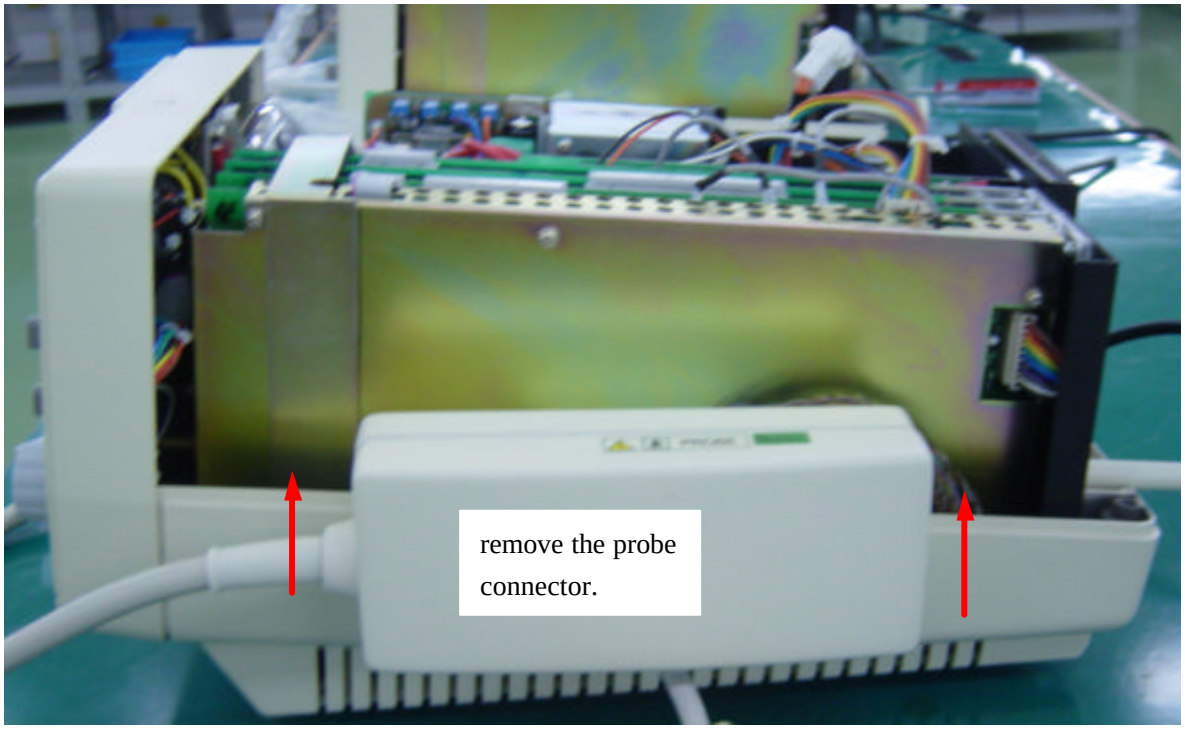
6. dismantle the screws, then remove EP-393200,EP-1894,EP-1895,EP-392800pc board.



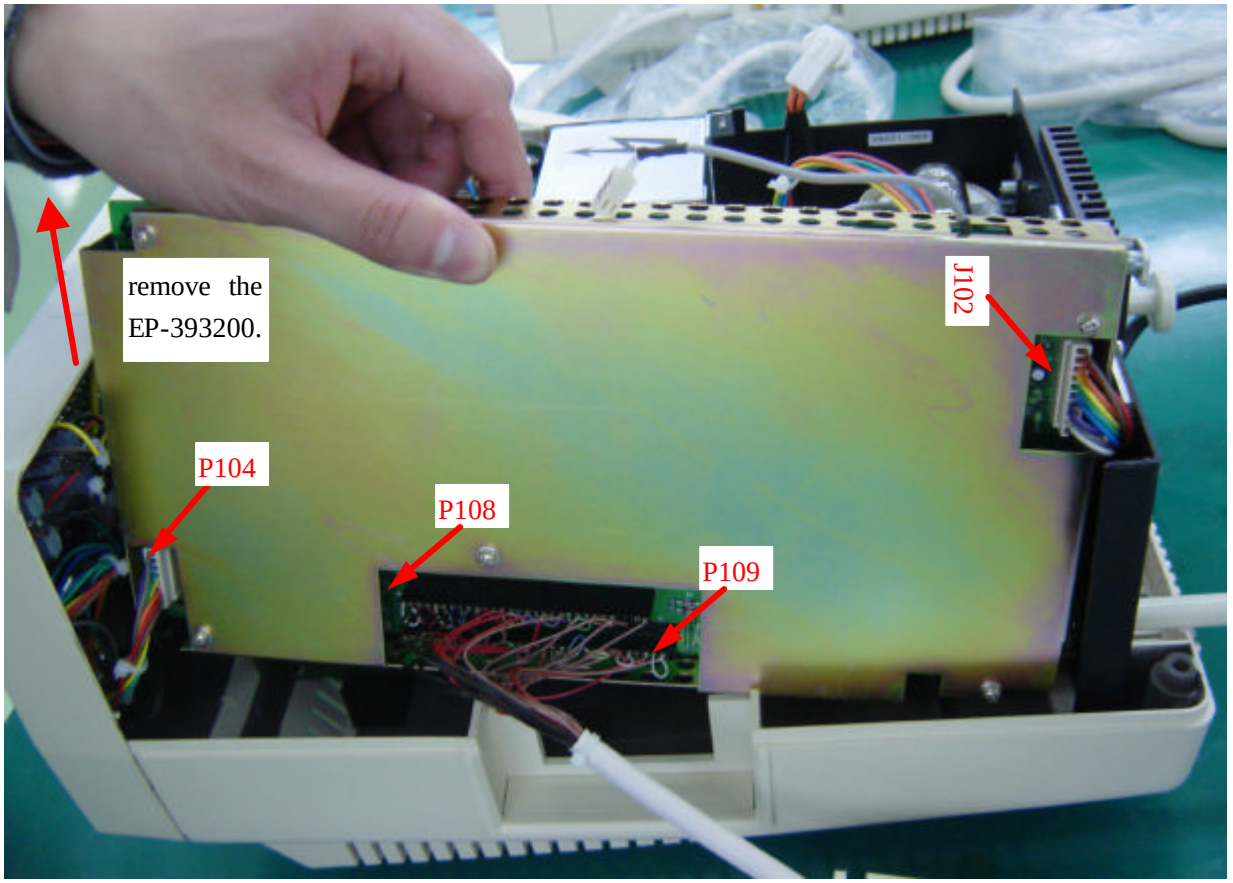
7. disconnect P108,P109,P104,P206,P204,P102, then EP-393200 can be removed；disconnect P201,P202,P203,P205, then EP-1894can be removed；disconnect P301,P302 then EP-1895 can be removed;
disconnect P402 then EP-392800 can be removed.



8．remove the probe connector.

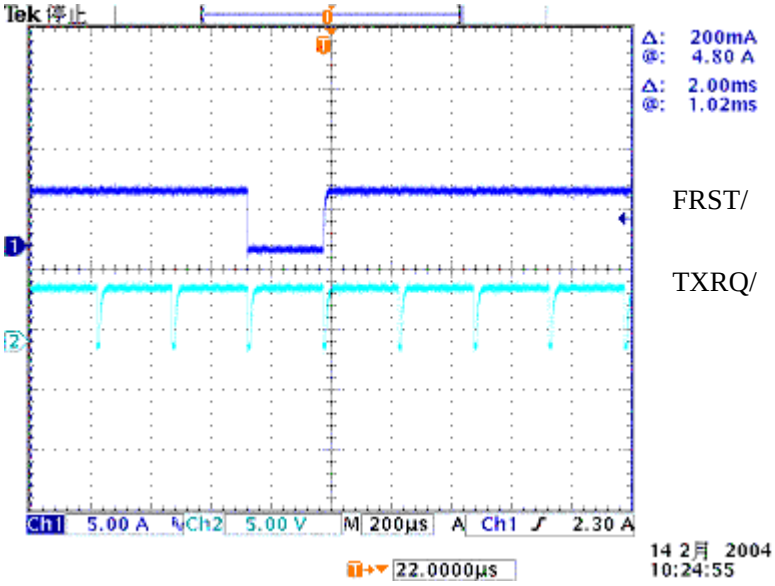


9．remove the EP-393200 (disconnect P108,P109,P104,P206,P204,P102 first).



SECTION 2. MAINTENANCE AND TROUBLESHOOTING

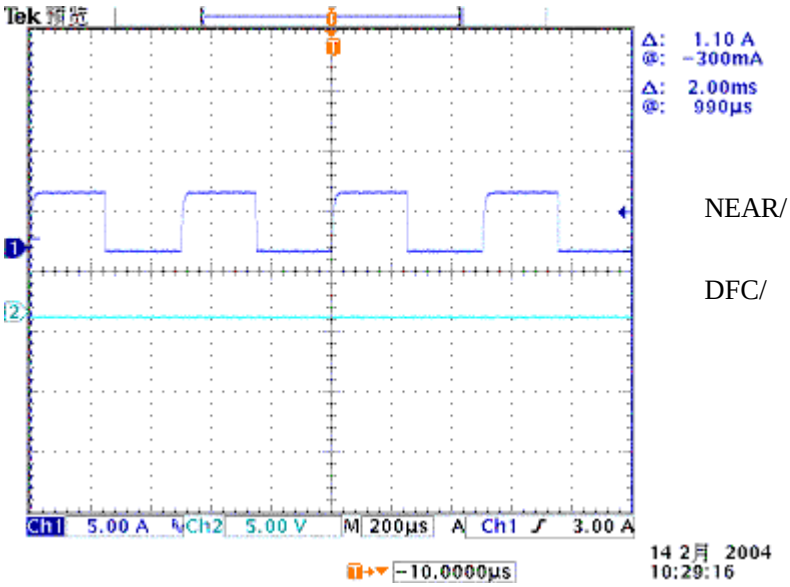
2-2. WAVE FORM DIAGRAM



FRST/ J105 ⑦

TXRQ/ J105 ⑤

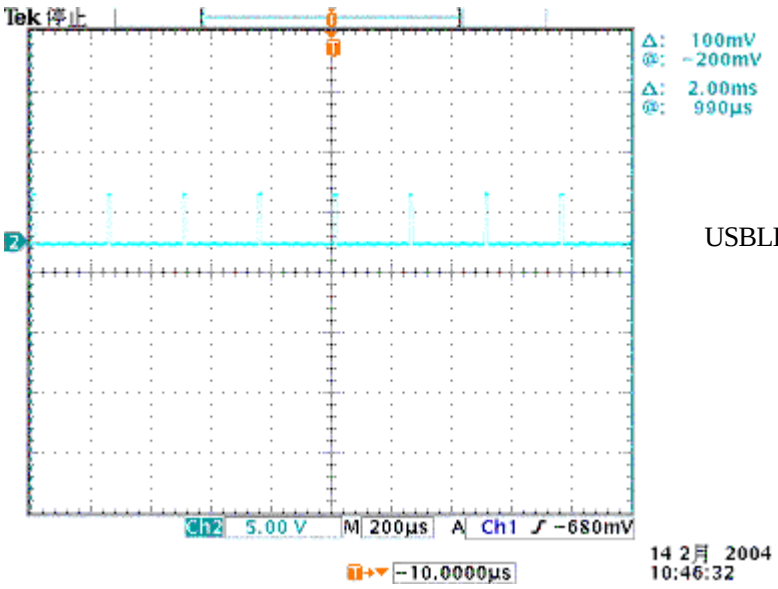
CONDITION) RATE:OFF DIST:OFF



NEAR/ J105 ③

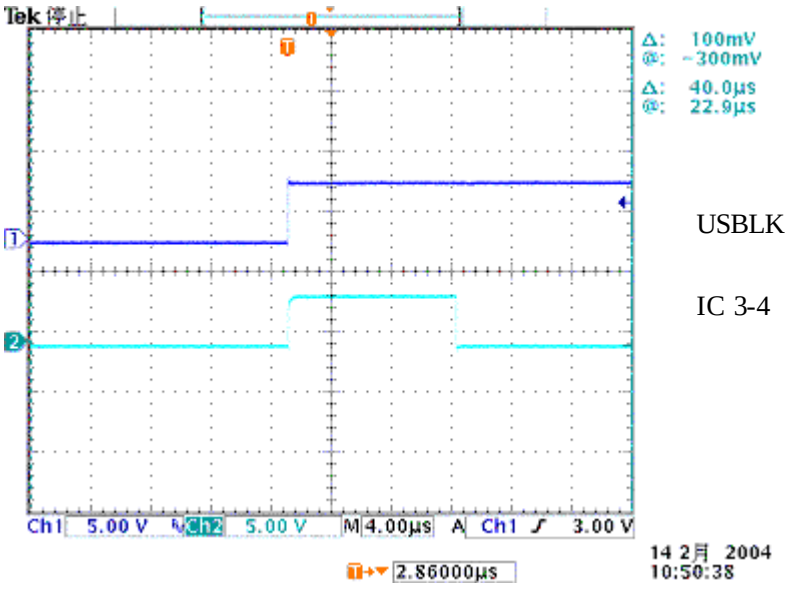
DFC/ J105 ①

CONDITION) RATE:OFF DIST:OFF



USBLK TP1

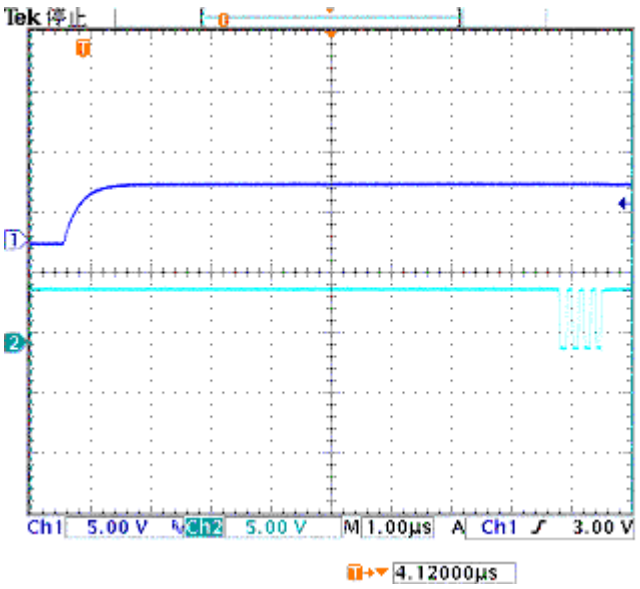
CONDITION) RATE:OFF DIST:OFF



USBLK TP1

IC 3-4

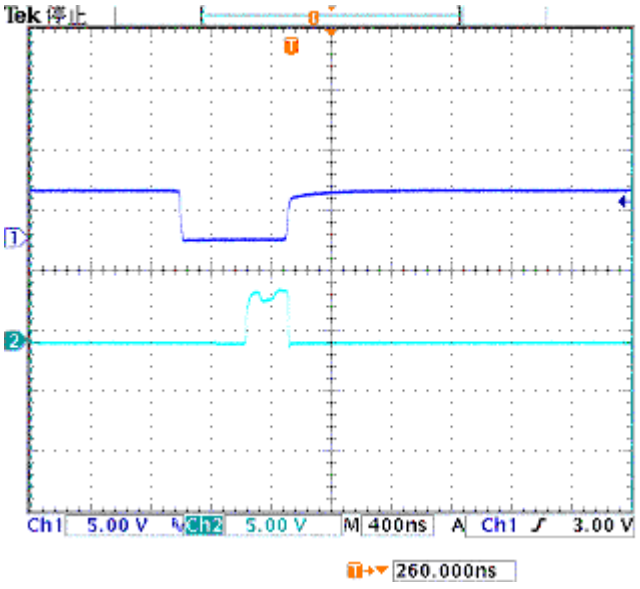
CONDITION) RATE:OFF DIST:OFF



IC 3-13

IC 6-1

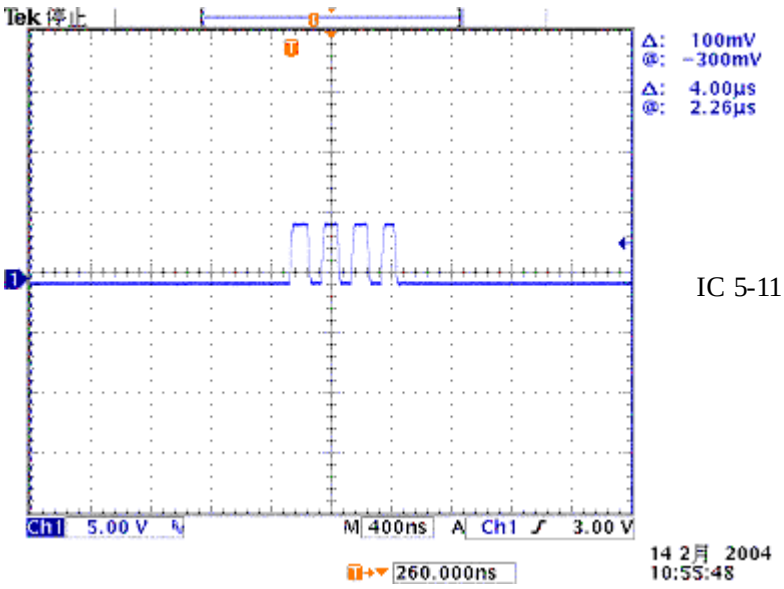
CONDITION) RATE:OFF DIST:OFF



IC 6-6

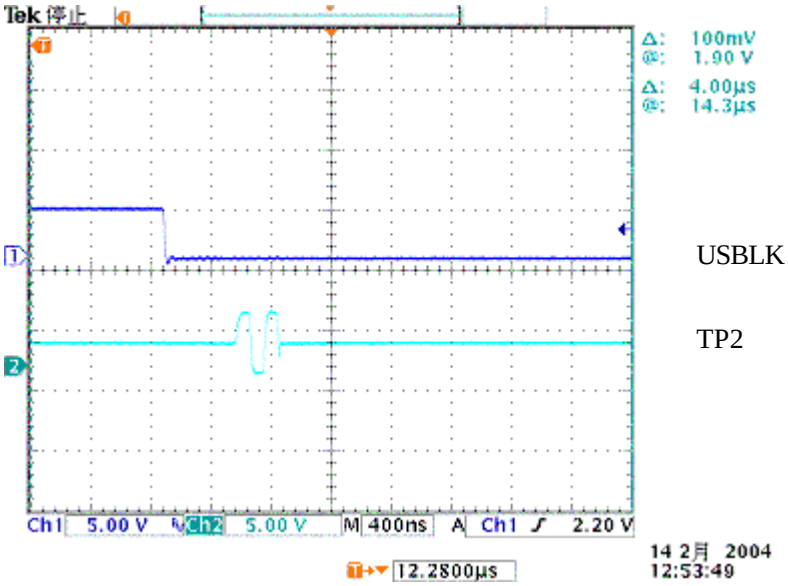
IC 6-8

CONDITION) RATE:OFF DIST:OFF



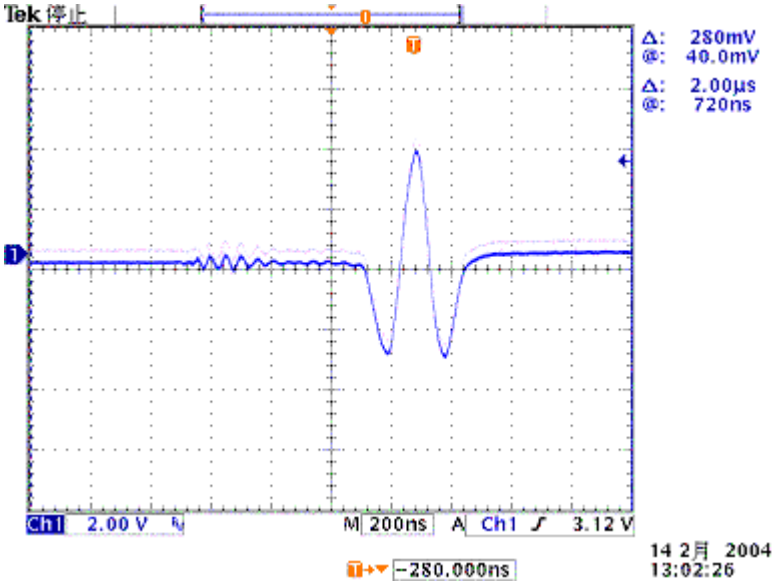
IC 5-11

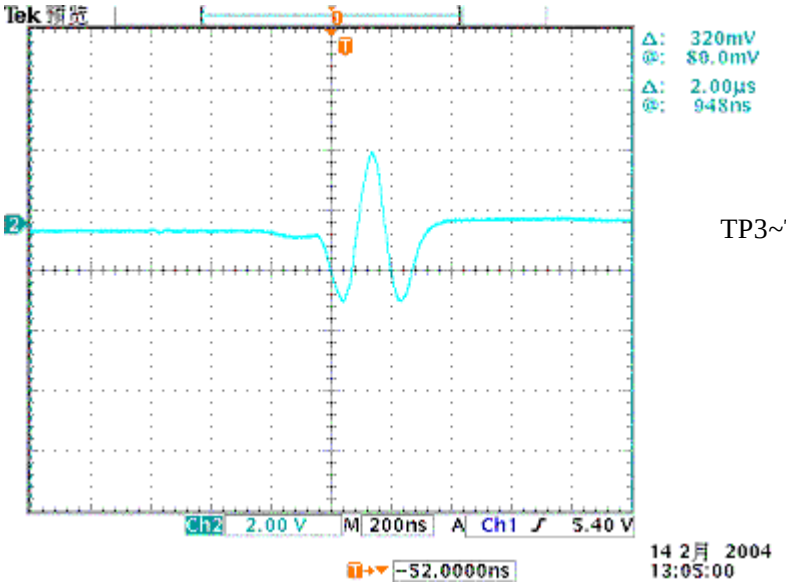
CONDITION) RATE:OFF DIST:OFF



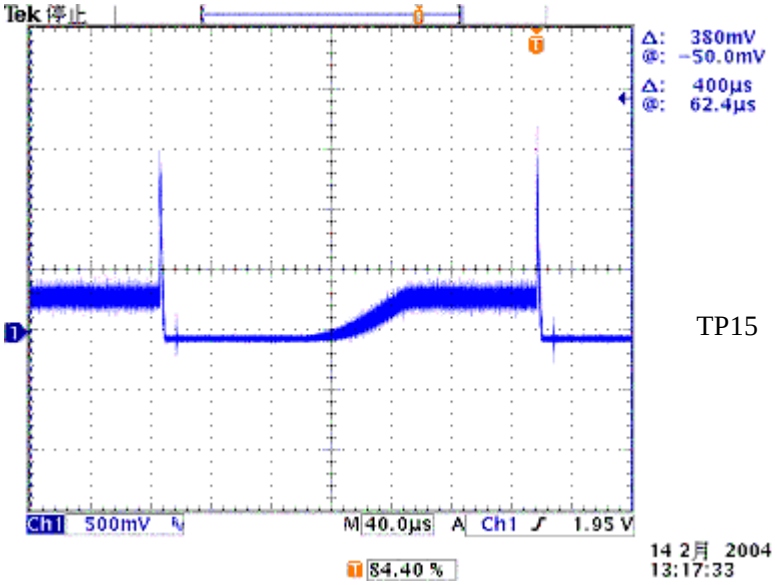
USBLK TP1

TP2


Tek 停止
Δ: 280mV
@: 40.0mV
Δ: 2.00µs
@: 720ns
Ch1 2.00 V
M 200ns A Ch1 3.12 V
-280.000ns
14 2月 2004
13:02:26

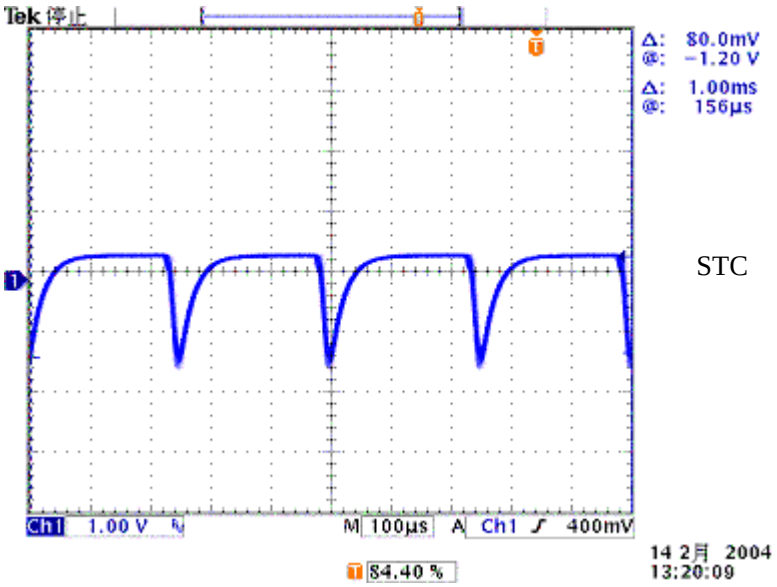

Tek 预览
Δ: 320mV
@: 80.0mV
Δ: 2.00µs
@: 948ns
Ch2 2.00 V
M 200ns A Ch1 5.40 V
-52.0000ns
14 2月 2004
13:05:00

TP3~TP10



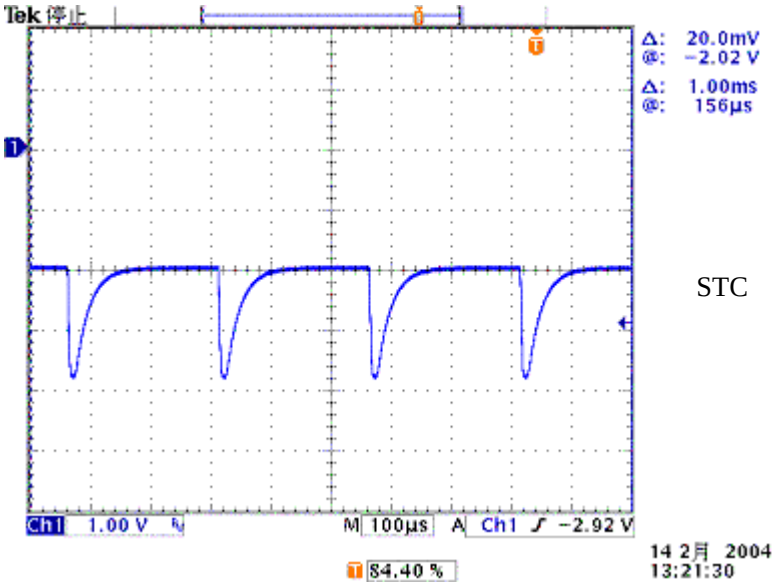
TP15

CONDITION) GAIN:MAX NEAR:MAX FAR:MAX



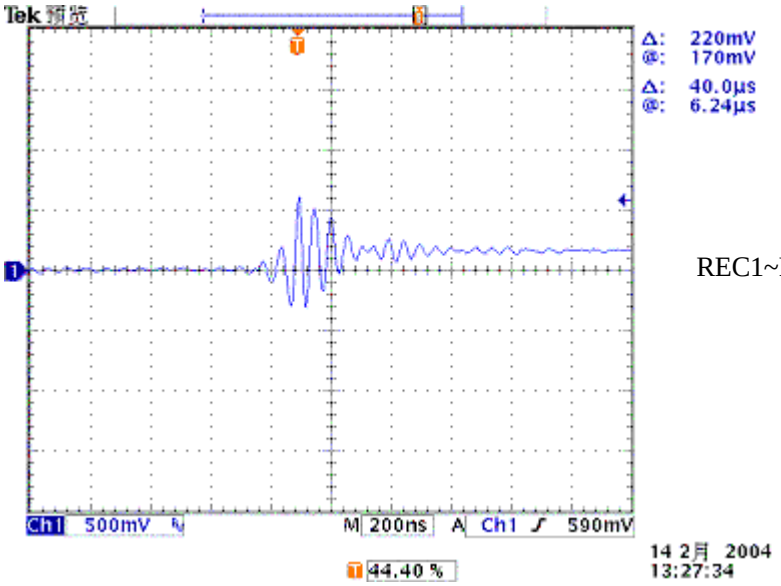
STC TP14

CONDITION) GAIN:MAX NEAR:MIN FAR:MIN RATE:UP

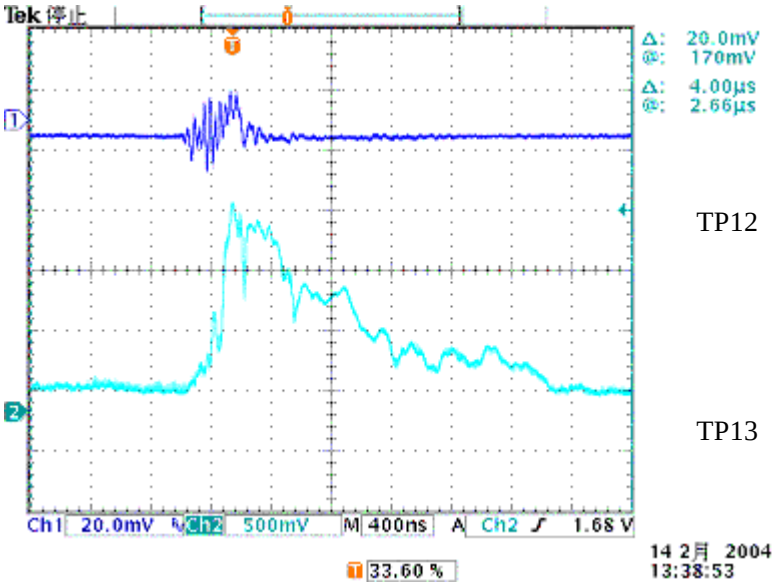


STC TP14

CONDITION) GAIN:MIN NEAR:MIN FAR:MIN RATE:UP



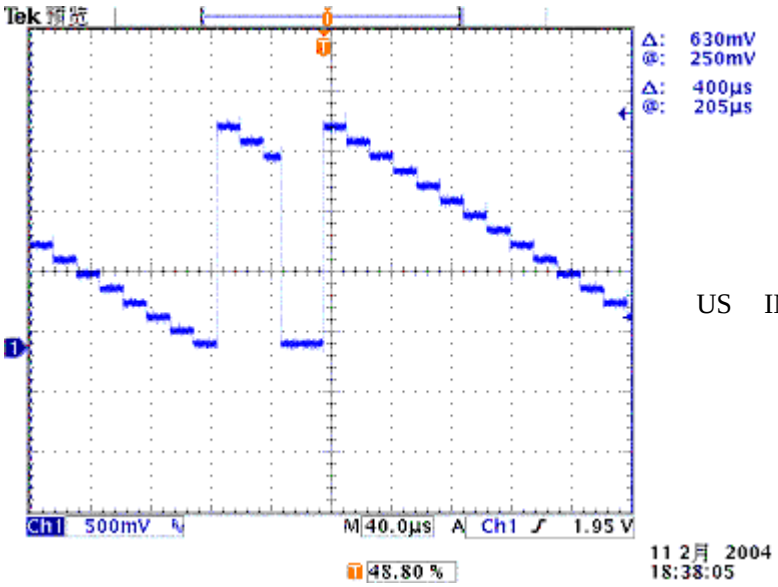
REC1~REC6 J109



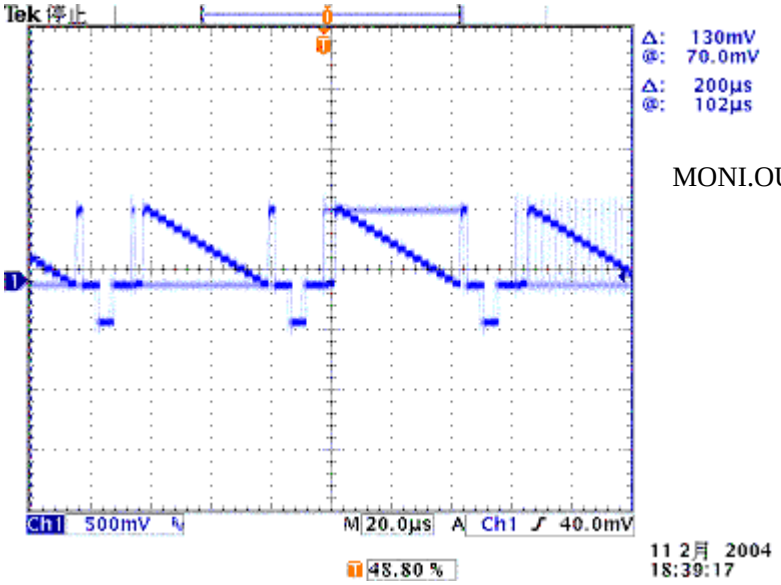
TP12

TP13

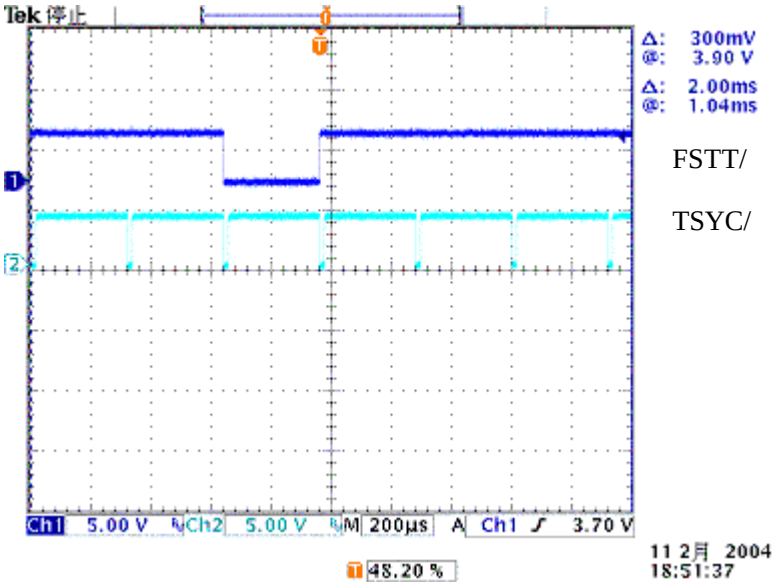
ADC & DAC EP-1894



US IN J204-①



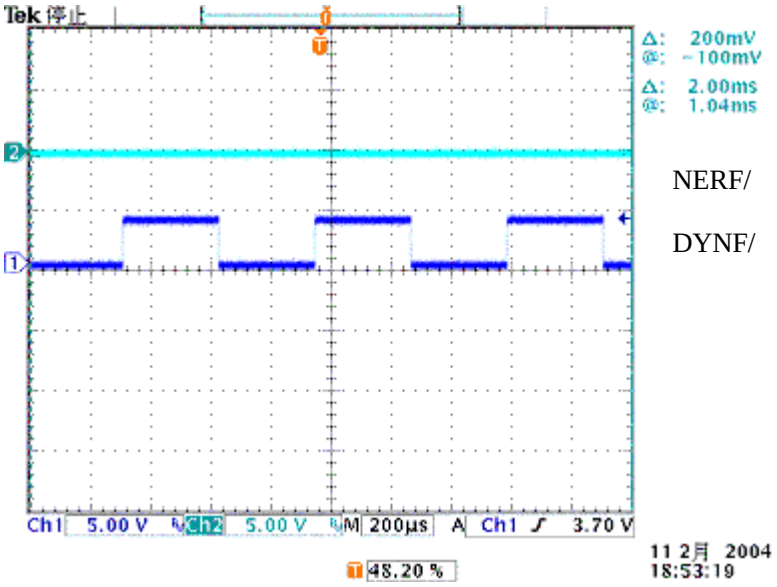
MONI.OUT　　J203-①



FSTT/　　IC1F-**9**

TSYC/　　IC1F-**5**

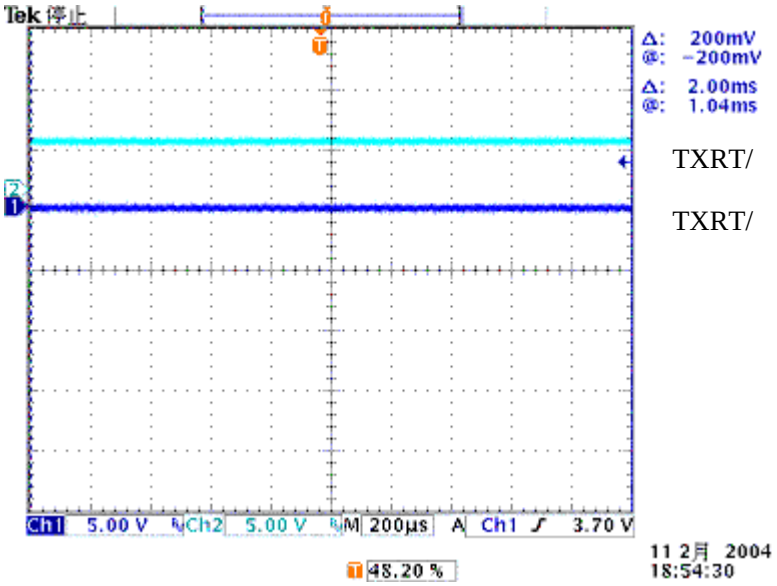
CONDITION)　RATE:OFF　DIST:OFF



NERF/ IC1F-**12**

DYNF/ IC1F-**2**

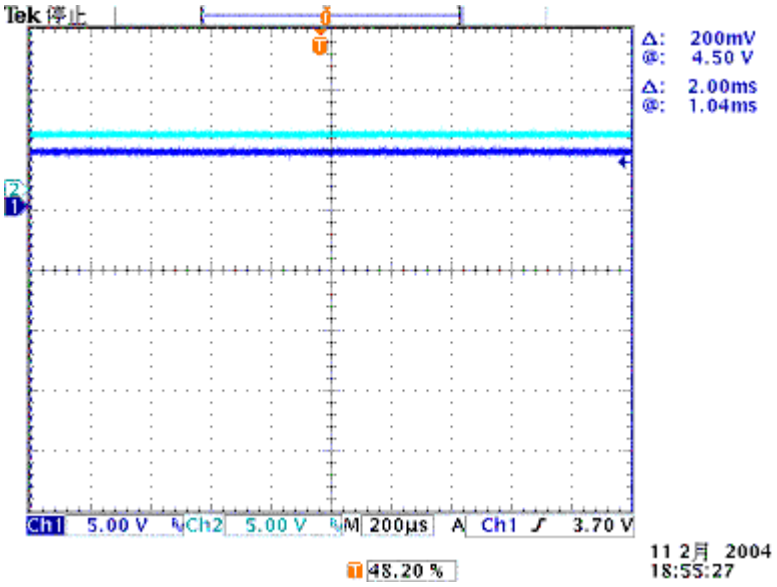
CONDITION) RATE:OFF DIST:OFF



TXRT/ IC1E-**2**

TXRT/ IC1E-**19**

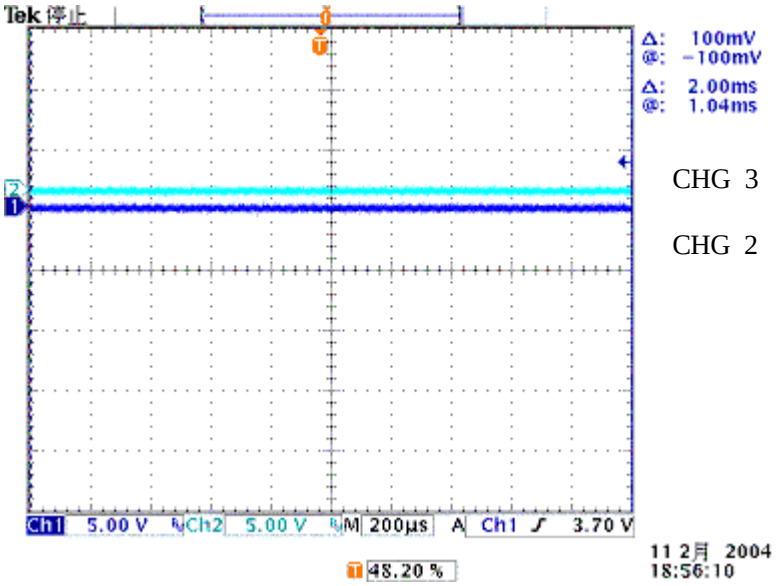
CONDITION) RATE:OFF DIST:OFF



CHG 5 IC1E-**16**

CHG 4 IC1E-**5**

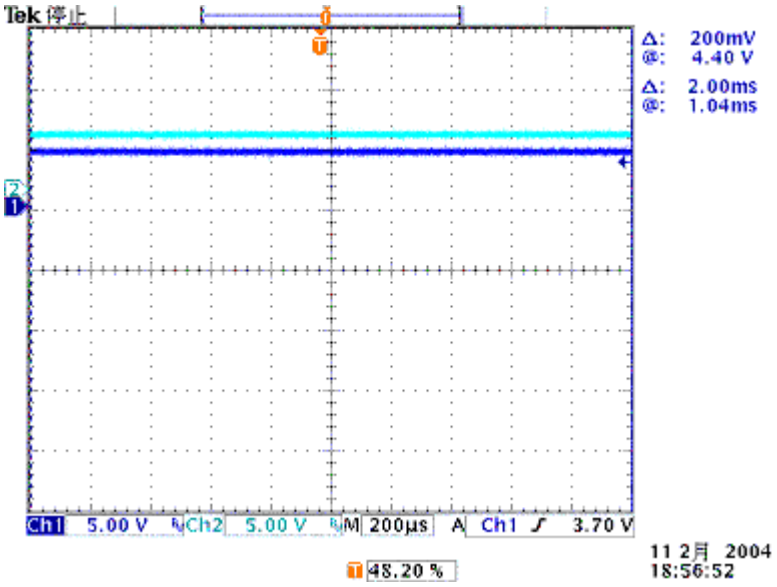
CONDITION) RATE:OFF DIST:OFF



CHG 3 IC1E-**9**

CHG 2 IC1E12

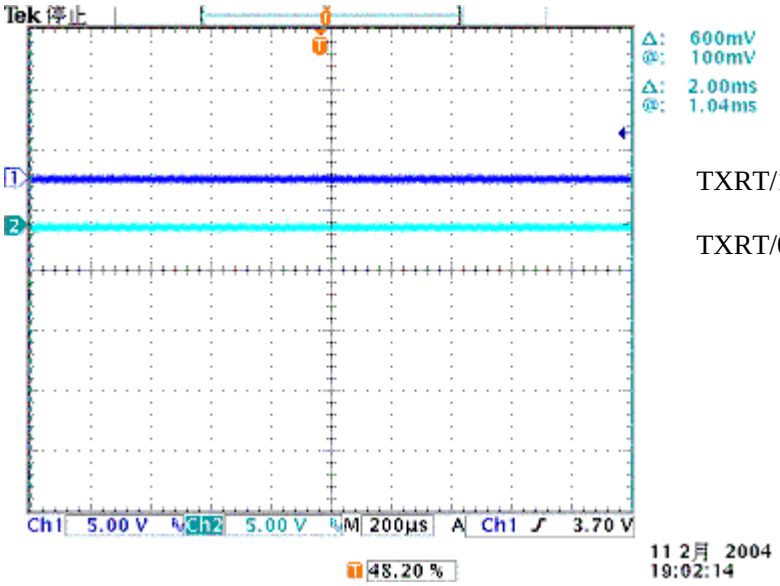
CONDITION) RATE:OFF DIST:OFF



CHG 1 IC1E-6

CHG 0 IC1E15

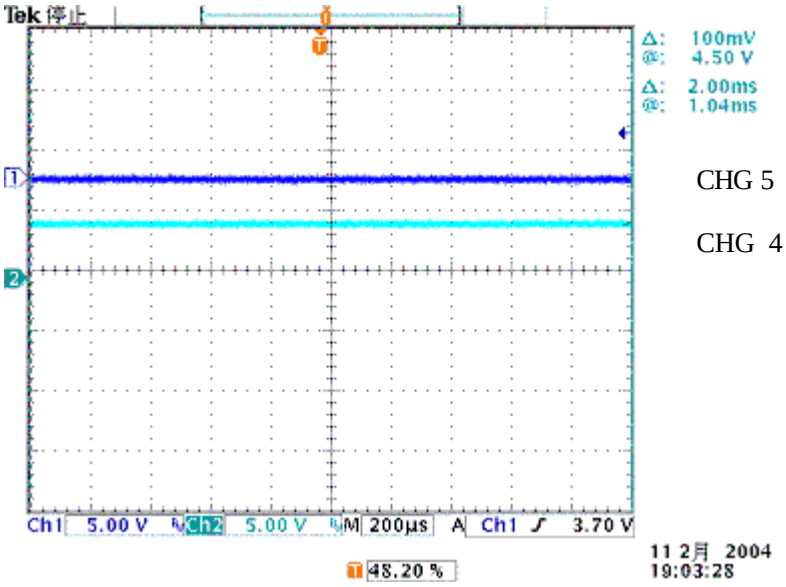
CONDITION) RATE:OFF DIST:OFF



TXRT/1 IC1E-2

TXRT/0 IC1E-19

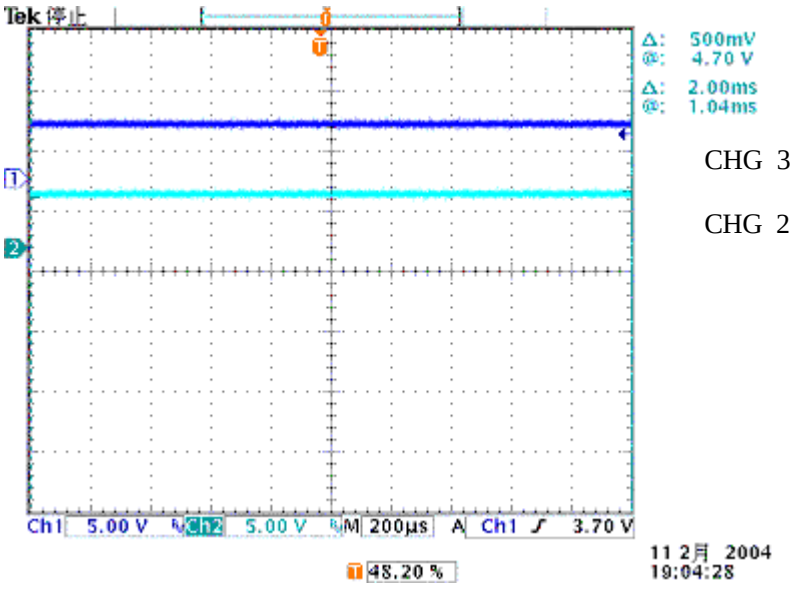
CONDITION) RATE:OFF DIST:LONG



CHG 5 IC1E-**16**

CHG 4 IC1E-**5**

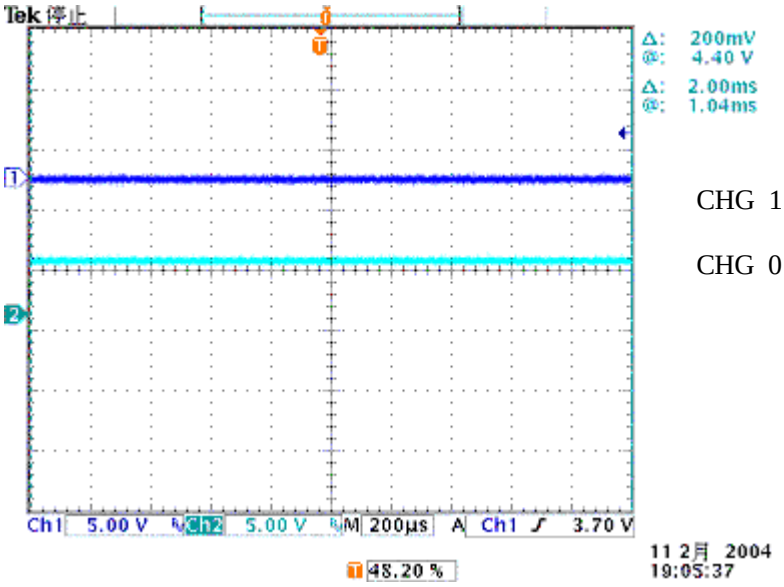
CONDITION) RATE:OFF DIST:LONG



CHG 3 IC1E-**9**

CHG 2 IC1E12

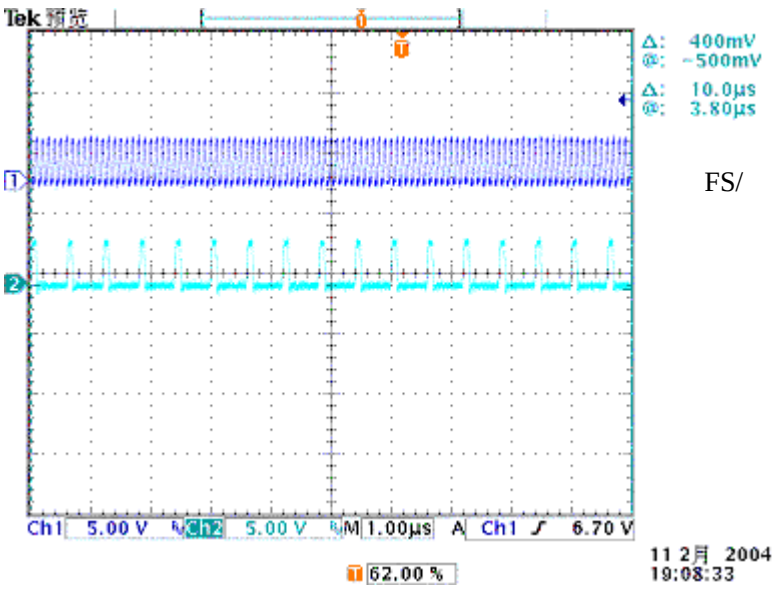
CONDITION) RATE:OFF DIST:LONG



CHG 1 IC1E-**6**

CHG 0 IC1E15

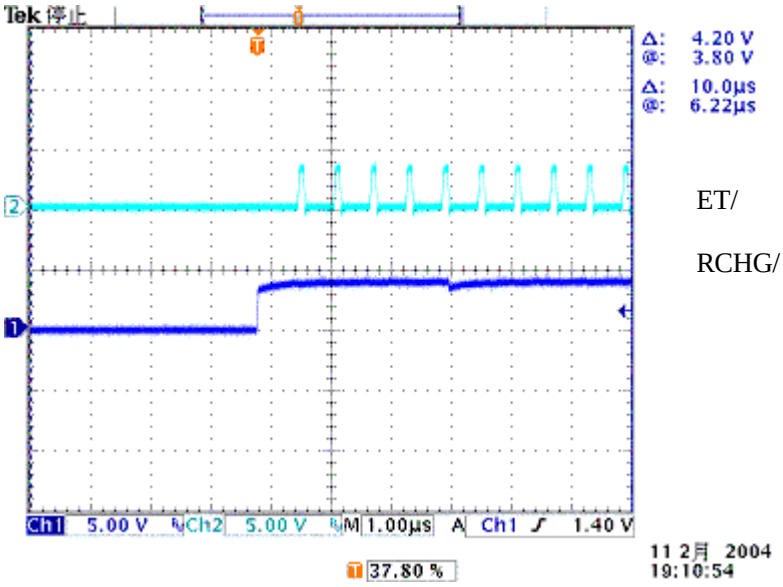
CONDITION) RATE:OFF DIST:LONG



FS/ IC1B-**11**

IC1A-**4**

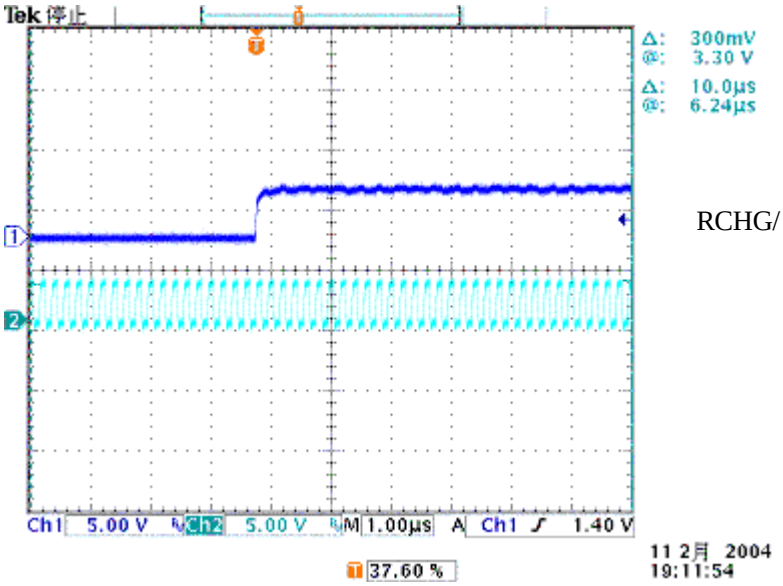
CONDITION) RATE:OFF DIST:OFF



ET/ IC1A-**2**

RCHG/ IC1A-**13**

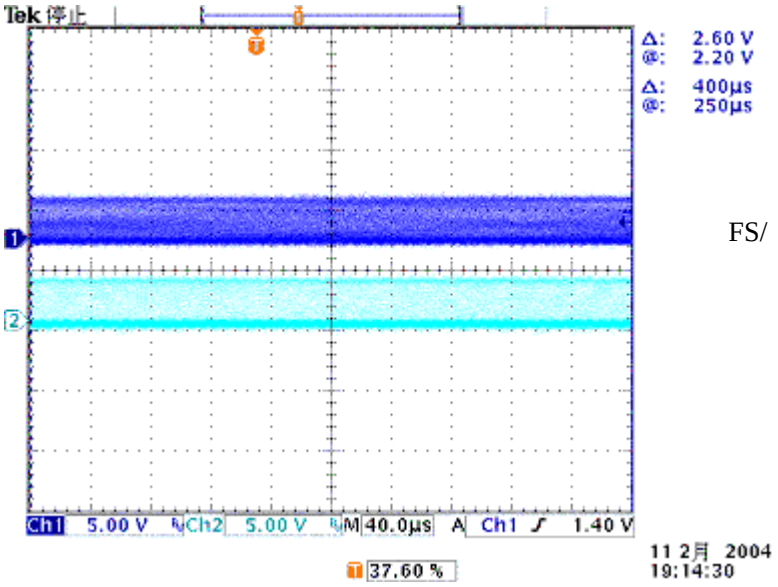
CONDITION) RATE:OFF DIST:OFF



RCHG/ IC1A-**15**

IC1A-**6**

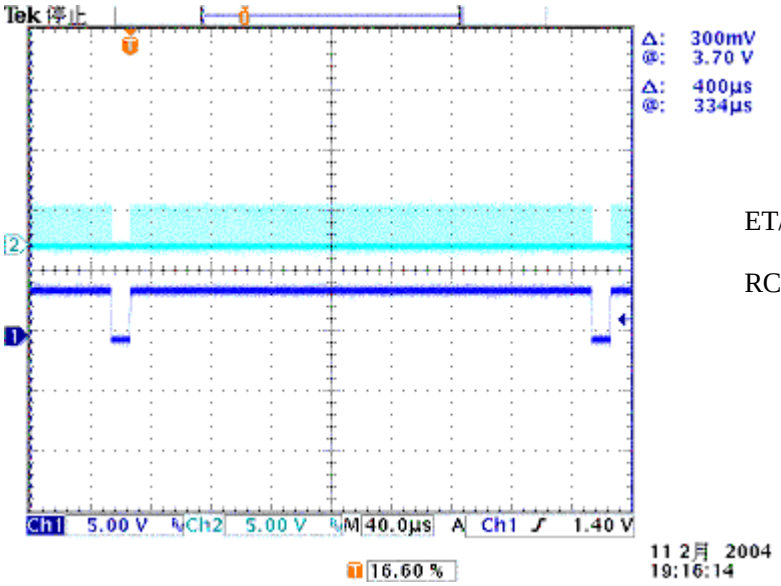
CONDITION) RATE:OFF DIST:OFF



FS/ IC1B-**11**

IC1A-**4**

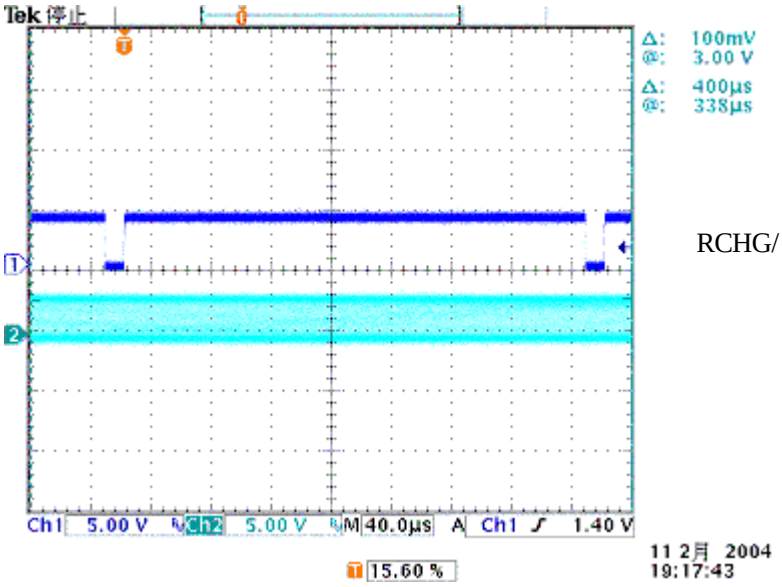
CONDITION) RATE:OFF DIST:OFF



ET/ IC1A-**2**

RCHG/ IC1A-**13**

CONDITION) RATE:OFF DIST:OFF

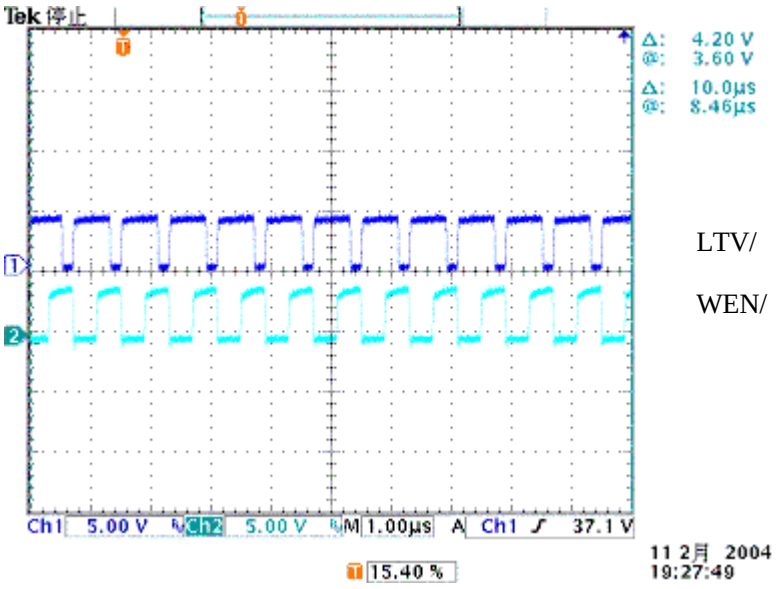


RCHG/ IC1A-**15**

IC1A-**6**

CONDITION) RATE:OFF DIST:OFF

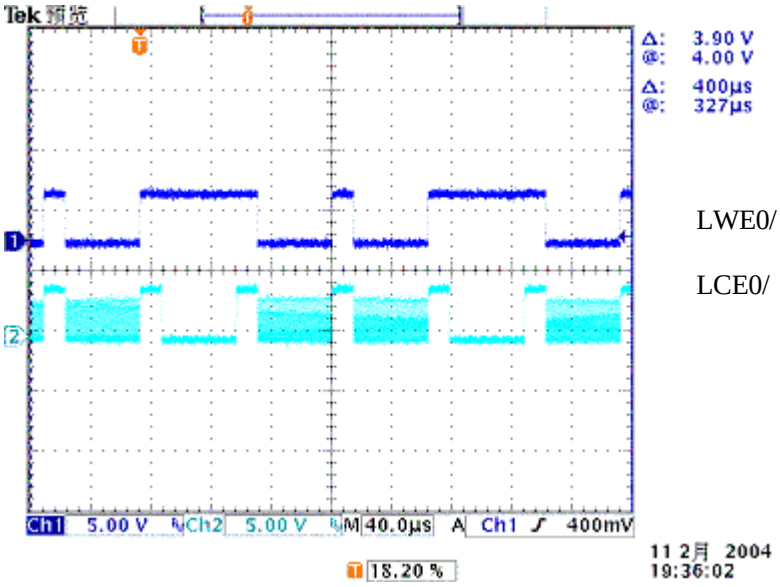
MEMORY EP-1895



LTV/ IC2D-**11**

WEN/ IC2D-**1**

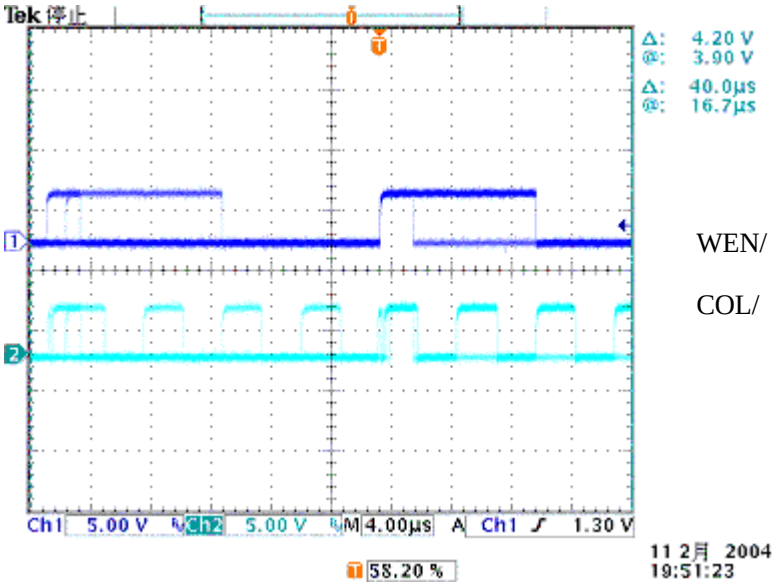
CONDITION) DIST:OFF



LWE0/ IC6F-**10**

LCE0/ IC6F-**8**

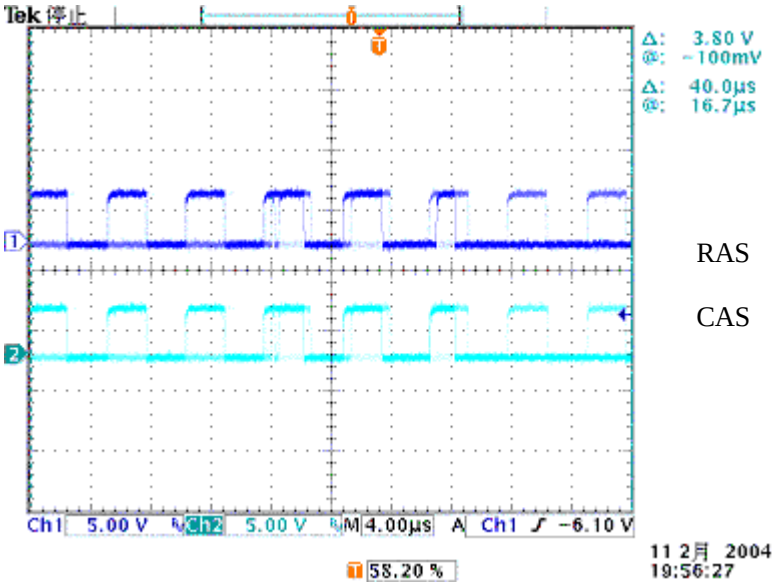
CONDITION) DIST:OFF



WEN/ IC7G-**6**

COL/ IC7F-**6**

CONDITION) DIST:OFF

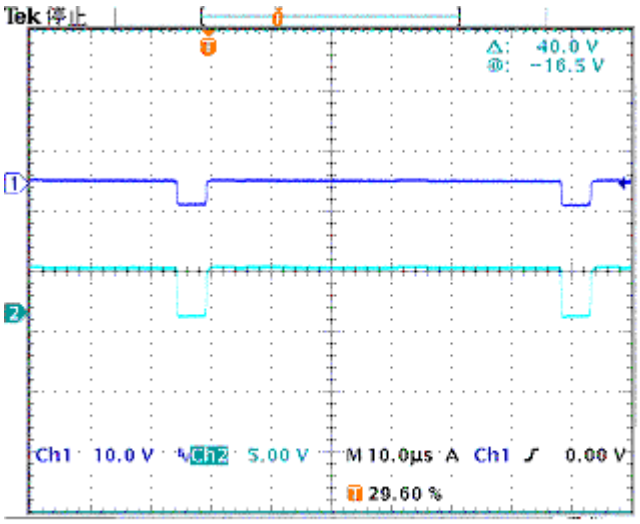


RAS IC7G-**1**

CAS IC7F-**10**

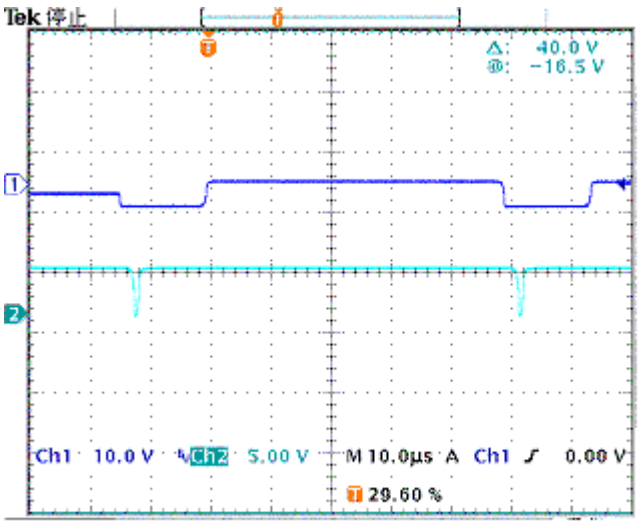
CONDITION) DIST:OFF

CONTROL EP-392800



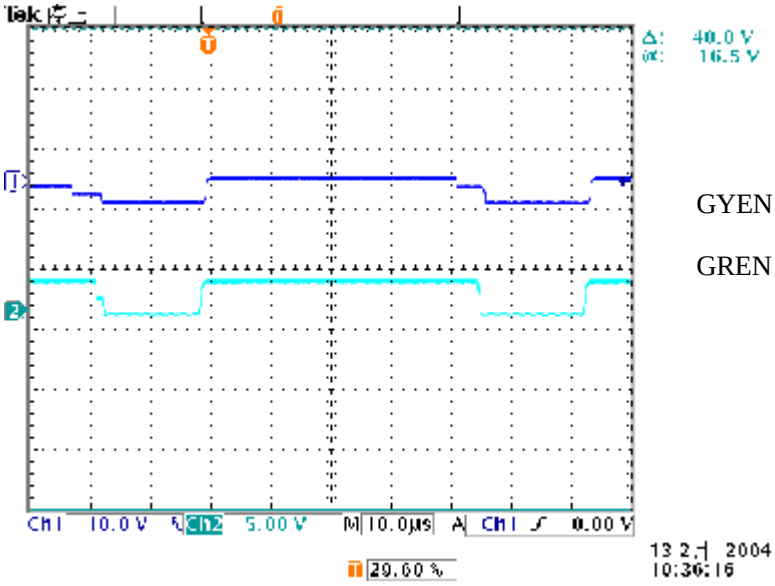
HRST/ IC7F-**12**

LMEN IC7F-**15**



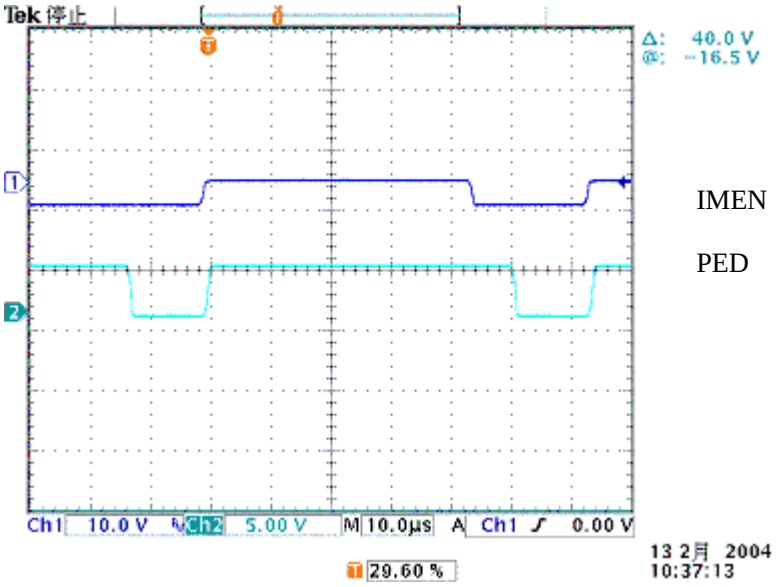
CBLK/ IC7F-**16**

CSYC/ IC7F-**19**



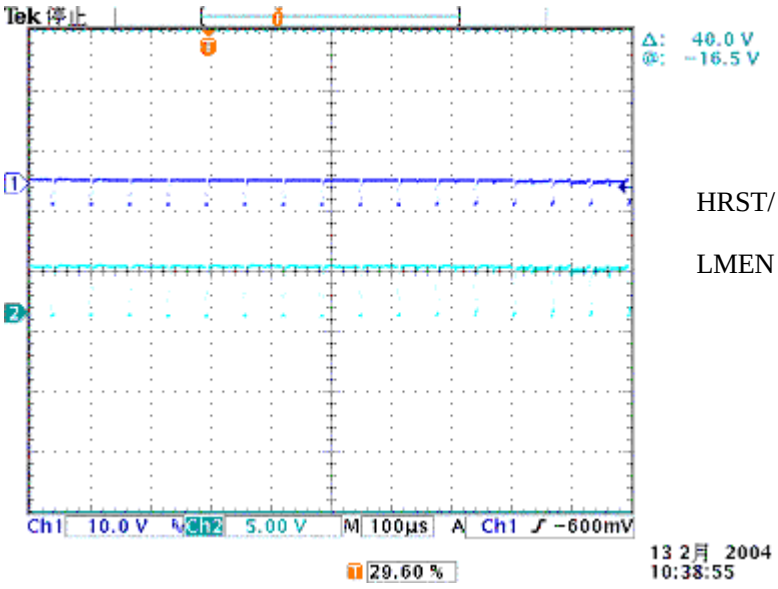
GYEN IC7F-**2**

GREN IC7F-**5**



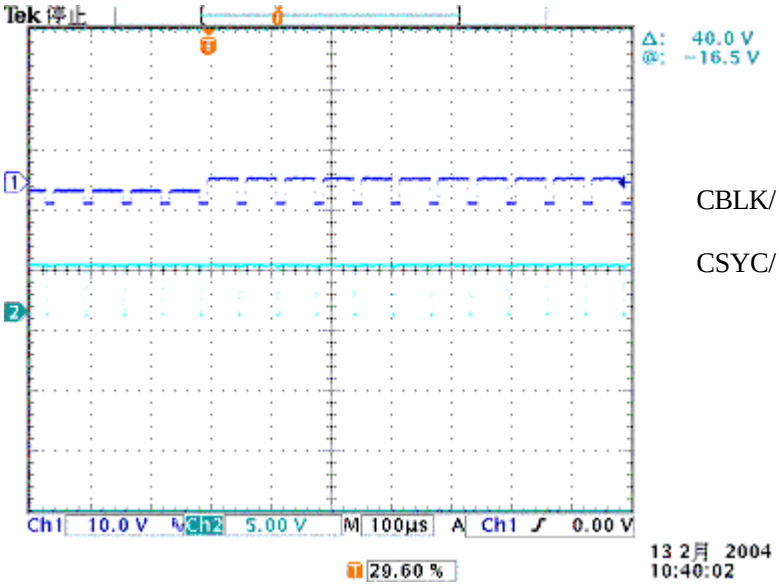
IMEN IC7F-**6**

PED IC7F-**9**



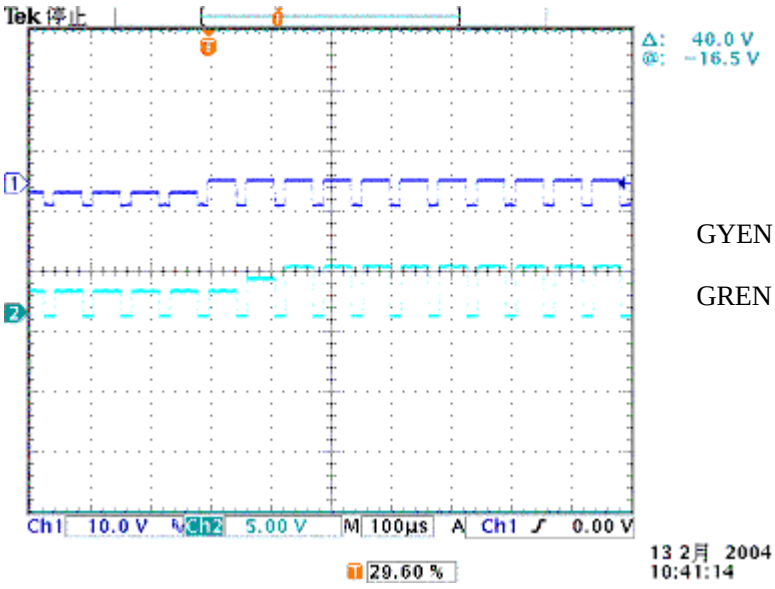
HRST/ IC7F-**12**

LMEN IC7F-**15**



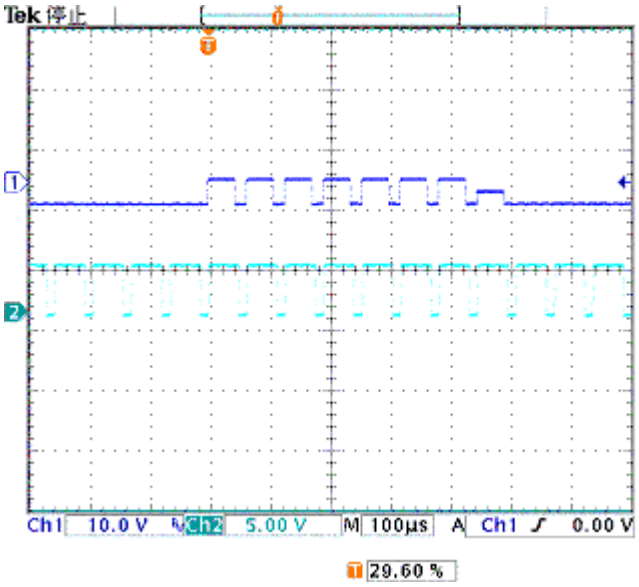
CBLK/ IC7F-**16**

CSYC/ IC7F-**19**



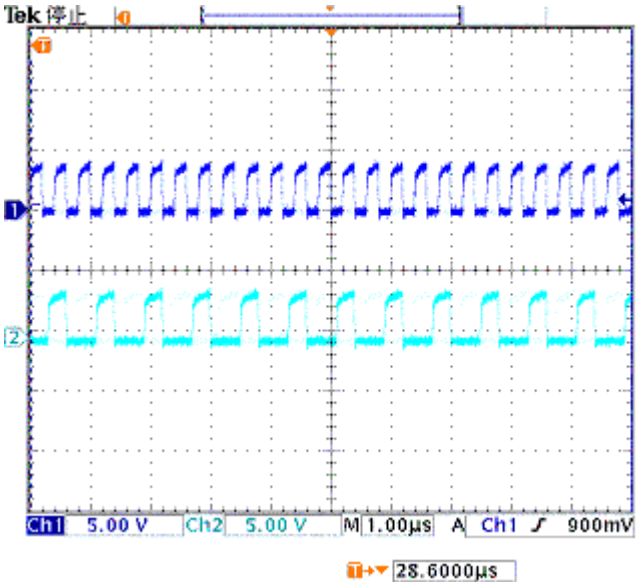
GYEN IC7F-**2**

GREN IC7F-**5**



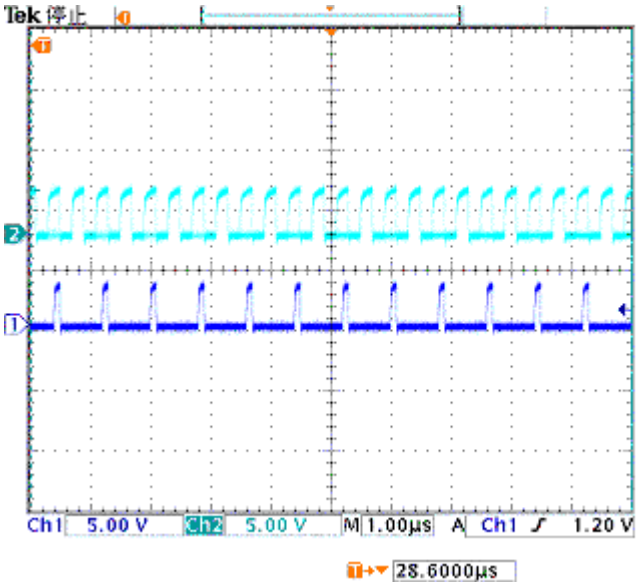
IMEN IC7F-**6**

PED IC7F-**9**



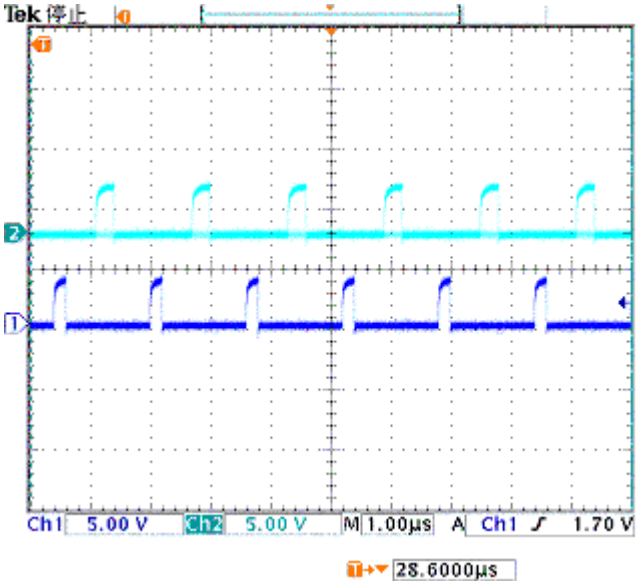
TRST IC6E-**12**

RAS IC6E-**15**



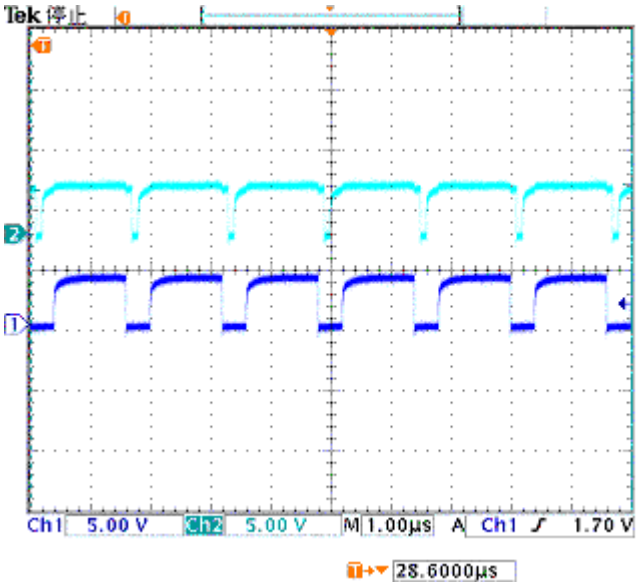
CAS IC6E-**16**

WE IC6E-**19**



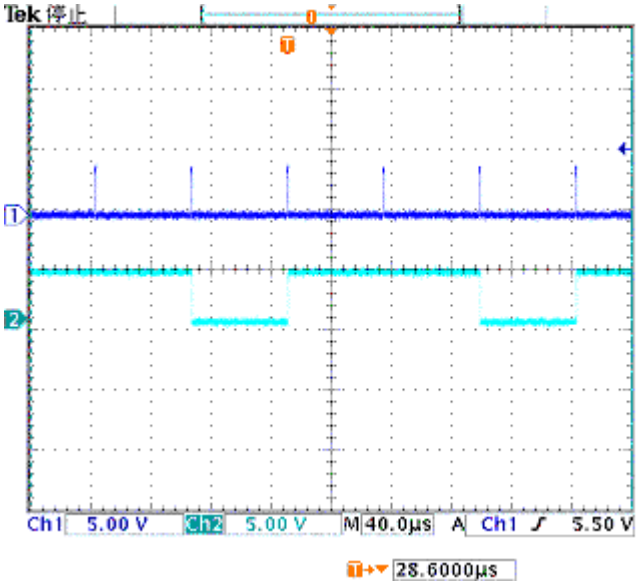
INH IC6E-**2**

SYC IC6E-**5**



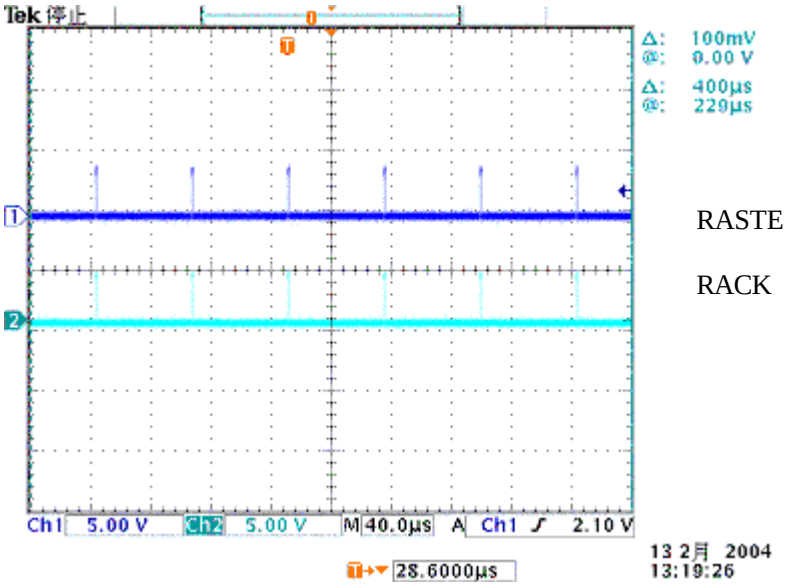
GMA IC6E-**6**

GWT IC6E-**9**



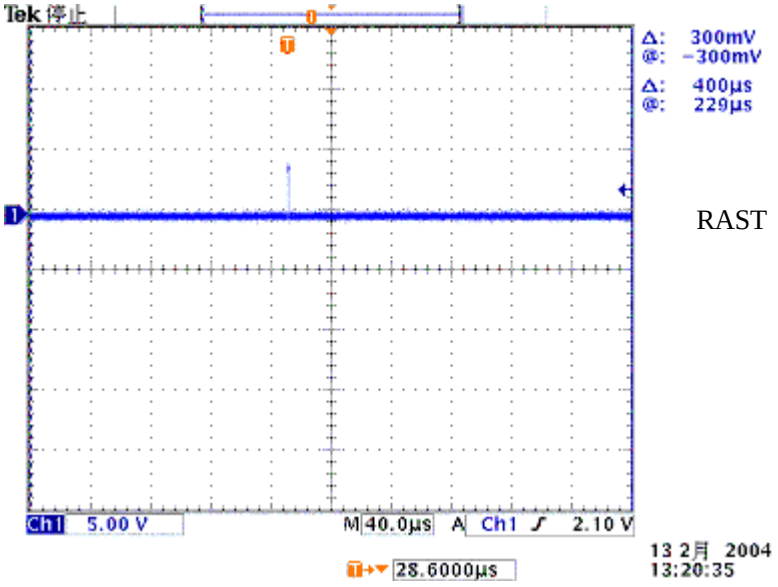
HRST IC7D-**1**

RACKE IC7D-**2**

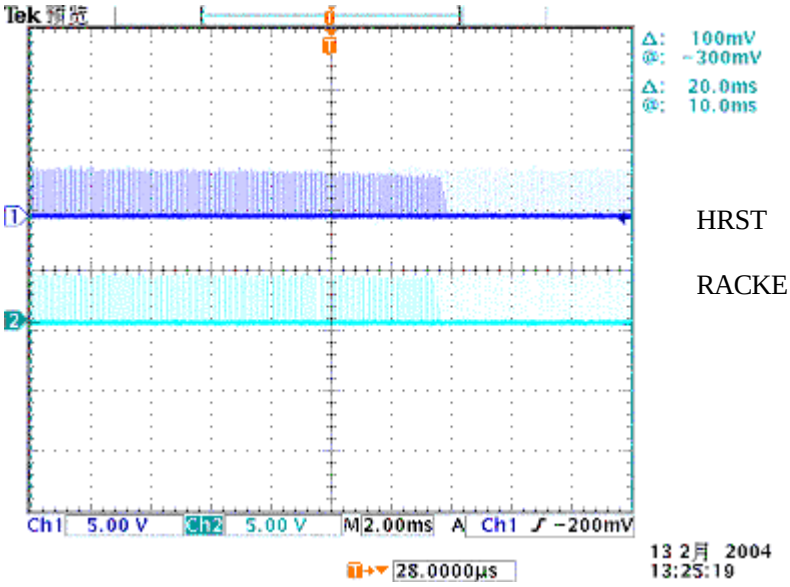


RASTE IC7D-**5**

RACK IC7D-**11**

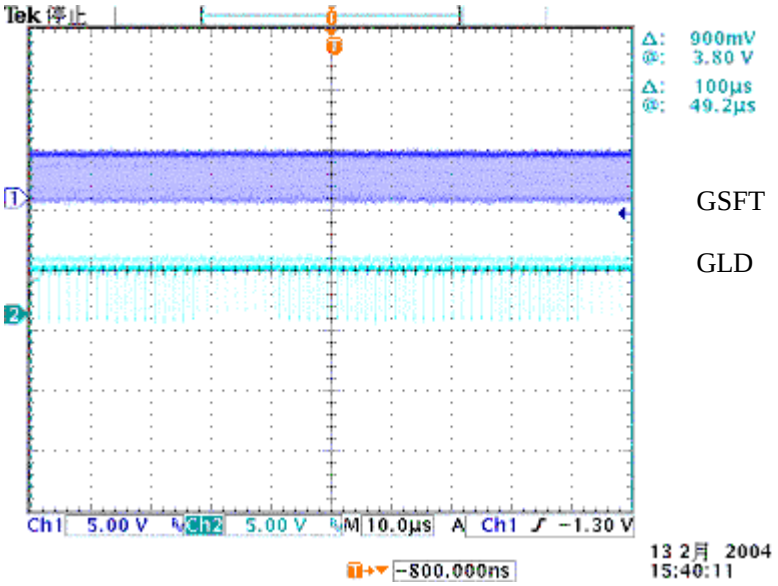


RAST IC7D-**8**



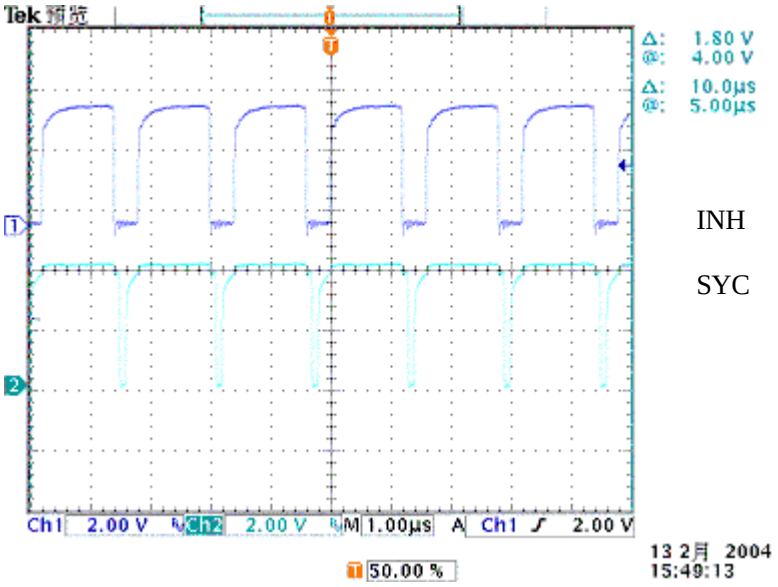
HRST IC7D-**1**

RACKE IC7D-**2**



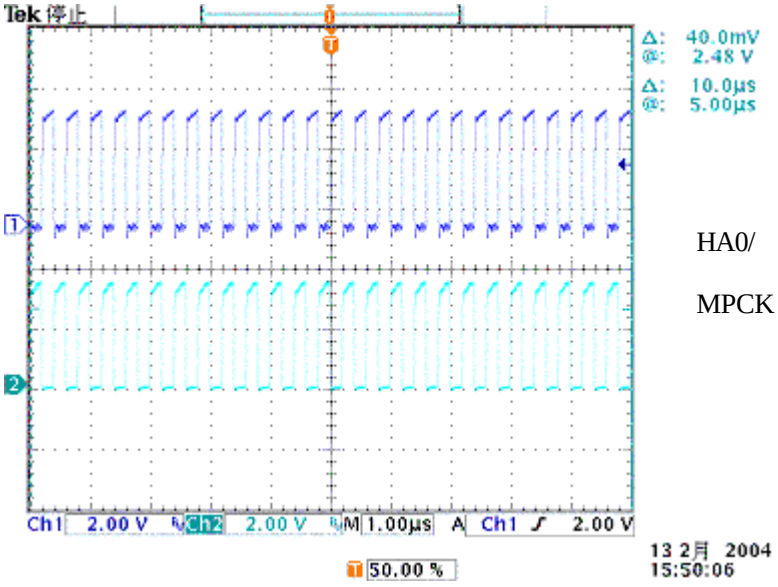
GSFT IC4D-**7**

GLD IC4D-**15**



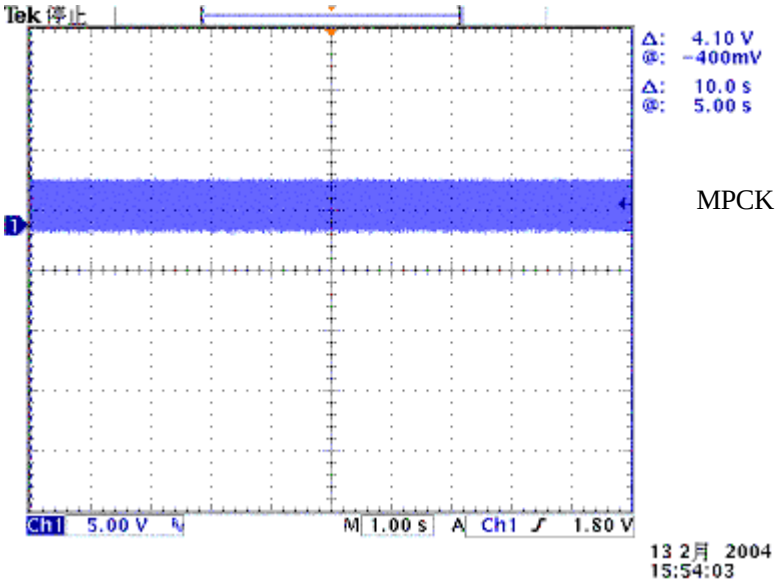
INH IC2D-**12**

SYC IC2D-**13**

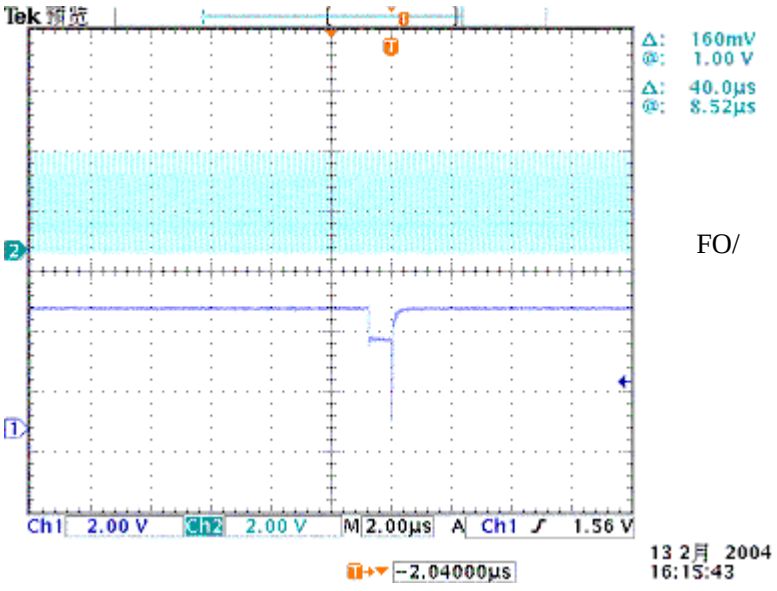


HA0/ IC2E-**10**

MPCK IC2E-**8**

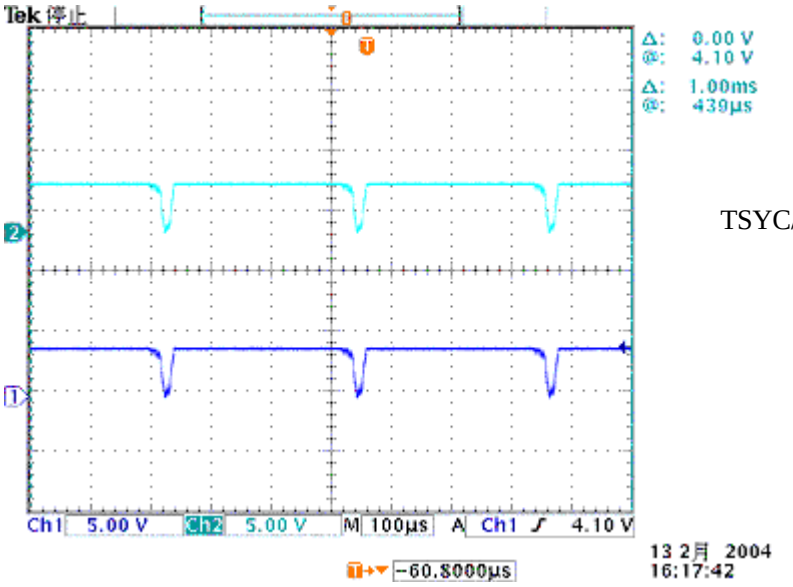


MPCK IC2A-**39**



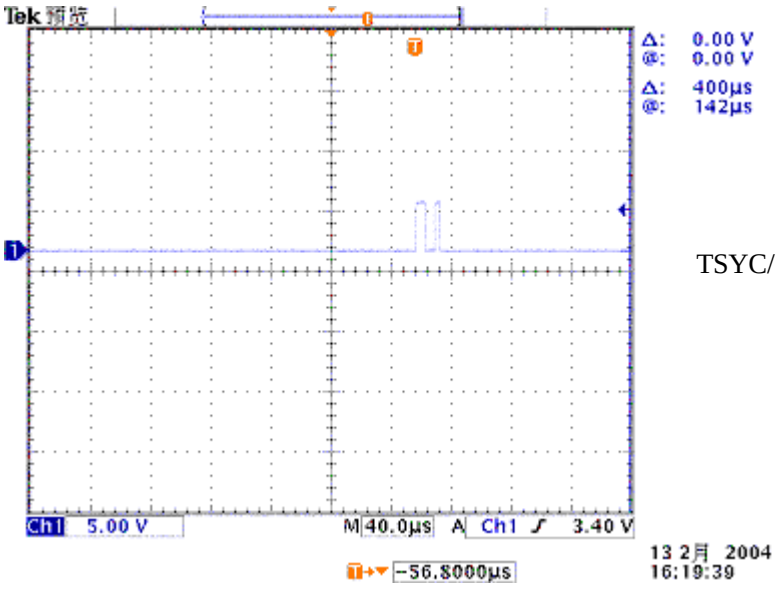
FO/ IC2B-**2**

IC2B-**6**



TSYC/ IC2B-**11**

IC2B-**12**



TSYC/ IC2B-**13**

SECTION 2. MAINTENANCE AND TROUBLESHOOTING

2-3. TROUBLESHOOTING

Troubleshooting

2-3-1 Troubleshooting policy

In the following the procedure to locate the trouble occurred in the equipment is described. In chapter 2-3-2 the trouble locating procedure for each unit is described. In chapter 2-3-3 faulty phenomena appeared on CRT are considerable to be defective and principal observing points are described. In chapter 2-3-4 the trouble shooting concerning to TV monitor is described.

Prior to commence the repair work, the followings should be checked:

(1) Mechanical damage on the equipment and cables.

(2) Connecting condition of the connectors, etc.

(3) Damage pf parts.

(4) Dust, water drop or other external causes.

Notices on repairman:

(1) In order to prevent circuit elements from damage, the power line should be OFF when cables and PCB are to be mounted or dismounted.

(2) Pay the utmost attention to the high potential at TV monitor.

(3) To observe the waveform, draw out the PCB and lay on in insulating sheet.

2-3-2 Procedure to Locate Trouble for Each Unit

The equipment consists of Power Supply unit, Ultrasound Picture Processor unit. Probe unit and TV Monitor unit. For each unit, trouble an be located as follow:

(1) Power Supply Unit

Confirm DC power supply voltage to be rated value as shown by Table2-3-1. If the power supply voltage is less than the rated value, separate the power supply circuit from other PCB and measure the voltage independently.

Thus the cause of the voltage drop, failure of the power supply circuit or other PCB. Can be judged.

(2) Ultrasound image processing block

The block is generally divided into two of Transmitter/Receiver unit (EP-393200) and D.S.C unit (EP-1894, EP-1895, EP-392800).

To the Transmitter/Receiver unit signals of TX RQ/, FR ST/, NEAR/ and DFC/ are sent from D.S.C unit through J105. Only the above four signals are the control signals(timing signals) sent to Transmitter/Receiver unit from outside.

By comparing those signals and output signal ECHO VIDEO(TP15) with the waveform in section2-3, it's possible to judge whether the falt is in Transmitter/Receiver unit or in D.S.C unit.

(3) Probe Unit

Confirm that ±5v, ±30v are supplied.

Confirm that the transmit trigger TRIG 1~8 and control signal CTRL 1~8 are input and observe the waveform of the received echoes REC 1~8 to judge the condition l~8 to judge the condition of

the probe. As it is difficult to judge the cause of the trouble such as loss of echo image, decreased sensitivity, noise, etc. only through the waveform observation, or to judge whether it is attributable to the probe or main body side, the test with a new probe is recommendable. To confirm the loss of echo image, the probe check methods as shown by Fig.2-3-1 is effective.
For the sensitivity check, RMI PHAMTOM Type 412, etc. are used and the sensitivity is judged from the tomogram..
When the probe is judged as failure, replacement of transducer or repayment inside the probe is impossible.

Table 2-3-1 DC POWER SUPPLY VOLTAGE

CONNECTOR NO.	DC VOLTAGE	SUPPLY TO	
J102 3 pin	+5V	MOS,H IC	EP-1893C
4	GND	LOG IC, OP AMP	EP-1671-1
J102 1	+5V	H IC	EP-1672-1
4	GND	LOG IC, OP AMP	(UST-5020)
J102 2	+12V		
4	GND		EP-1893C
J102 7	-12V	H IC	
4	GND		
J102 5	+30V		EP-1671-1
4	GND	H IC	EP-1672-1
J102 9	-30V	MULTIPLEXER	(UST-5020)
4	GND		
J201 1	+5V	A/D CON, D/A CON	
6	GND	TTL, OP AMP	
J201 5	-5V	A/D CON, D/A CON	EP-1894
6	GND	OP AMP	
J201 2	+12V	A/D CON, D/A CON	
6	GND	MOS	
J301 5	+5V	TTL, MEMERY	EP-1895
3	GND	ROM	
W1 4	+12V	TV-MONITOR	PC0017
3	GND		

Probe check

1. Apply ultrasound jelly on surface of probe, then set a coin and move slowly in the surface.

2. ECHO slide aside on the screen according to the coin. ECHO should not leap nor appear at two position or more.

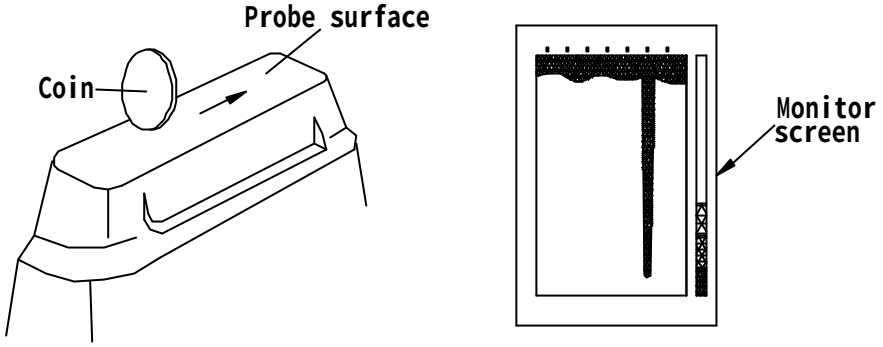
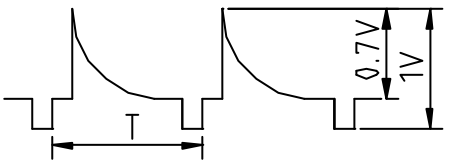


Fig. 2-3-1 PROBE CHECK

Table 2-3-2 MONITOR INPUT SIGNAL

CONNECTOR NO.	SIGNEL
UPC-1366A w1 1pin 2pin (GND)	 T=63.5us (525 Lines) T=64us (625lines)
w1 4pin 3pin	+12V DC GND

(4) TV Monitor Unit

As a DC coupled monitor is adopted, the screen does not brighten at all. Unless the composite

video signal is input or video component is not included in the composite video signal.
If the image does not indicate properly even when the input signals of PC0017 “W1” on IP-0503-TV are recognized +12V and composite video as shown in Table 2-3-2, The monitor unit should be judged as failure.

2-3-3 Classifies troubleshooting methods by the case of trouble. This section consists of as follows:
1) Symptom:……Describes symptom of trouble.
2) Cause of failure……...Lists the unit or PCB that is considered to be defect.
3) Main points of checking……Lists the points to be checked for judgment of faulty PCB.
* Refer also to section2-2 “Waveform diagrams”

Phenomena which are not considered as faults under special condition.

It rarely happens that because of instantaneous power interruption or great drop down of power voltage (-10% or lower), panel switches does not operate correctly. This is caused by abnormal operation of microprocessor, due to lowered power voltage.
To restore the condition, turn off the power once and after two or three seconds turn on the power again. The above condition occurs due to the characteristic of the circuit and it’s not considered as a fault.
However if the normal operation cannot be restored when the power is turned on again, it is a fault.

TROUBLE OF WHOLE IMAGE ON MONITOU SCREEN

EX.1 1) symptom: Nothing appears on the screen.

2) Causes of failure:
Failure of ±5V, +12V Power supply (EP-1882)
Failure of composite VIDEO (EP-1894)
Failure of TV-Monitor (IP-0503-TV)
Breakage of the cable or contact failure of connector.

3) Main points of checking:

EP-1882 J502 ±5V DC +12VDC

EP-1894 J203 1 PIN (MONI.OUT)

TV-Monitor → Refer to chapter 2-3-4 IP-0503-TV troubleshooting.

EX.2 1) symptom:

Ultrasound image, scale marker and gray scale bar are not displayed, unless raster bright on the screen

2) Causes of failure:

System clock generator does not generate Fs nor Fo. (EP-1895)

Defect of A/D Converter circuit (EP-1894)

Failure of TV-Monitor

3) Main points of checking:

EP-1895 IC1F 8 pin (FO)

EP-1894 J203 1 pin (MONI.OUT)

TV-Monitor → Refer to chapter 2-3-4 IP-0503-TV troubleshooting.

EX.3 1) symptom:

Picture is displayed in disorder, or picture flows on the monitor

2) Causes of failure:

Level of TV-signal is low or too high. (EP-1894)

Sync failure of TV-Video signal (EP-392800)

System clock generator dose not generate stable clock.

3) Main points of checking:

EP-1894 J203 1 pin (MONI.OUT)

EP-1895 IC1F 8 pin (FO)

TROUBLE OF ULTRASOUND IMAGE

EX.4 1) symptom:

Raster, scale marker and gray scale bar are displayed, but Ultrasound image is not displayed on the screen.

2) Causes of failure:

Failure of ±30V, -12V Power supply (EP-1882)
Failure of Probe (UST-5813-5)
Defect of Tx & Rx circuit (EP-393200)
Defect of A/D Converter circuit (EP-1894)
Defect of Image memory circuit. (EP-1895)

3) Main points of checking:

EP-1882 J502 ±30V DC -12VDC
EP-1882 J502 P102
EP-393200 TP3~TP10 (TRIG 1~TRIG 8)
EP-393200 IC23~IC30 each 3 pin (REC 1~REC 8)
EP-393200 TP15 (ECHO VIDEO)
EP-1894 Out of A/D Converter IC6A 2,5,7 pin
EP-1894 Data line of echo video data
EP-1895 Data line of echo video data

EX.5 1) symptom:

At a certain part of the Ultrasound image area, sensitivity is excessively low or not at all.

2) Causes of failure:

Defect of Tx & Rx phase control circuit (EP-393200)
Failure of Probe (UST-5813-5)

3) Main points of checking:

EP-393200 IC14 (CTRL1~CTRL8)
EP-1894 IC13 (CTRLA~CTRLD)

EX.6 1) symptom:

Sensitivity of whole Ultrasound image is excessively low.

2) Causes of failure:

Failure of ±30V Power supply (EP-1882)
Defect of Tx & Rx Control circuit (EP-393200)
Defect of Receiving circuit (EP-393200)
Defect STC circuit (EP-393200)
Failure of Probe (UST-5813-5)

3) Main points of checking:

EP-1882 J502 ±30V DC
EP-393200 TP3~TP10 (TRIG 1~TRIG 8)
EP-393200 TP15 (ECHO VIDEO)
EP-393200 TP14 (STC OUT)

EX.7 1) symptom:

When probe is touched, indication of noise is increased.

2) Causes of failure:

Poor shielding of Probe (UST-5813-5)
Breakage of cable or contact failure of Probe (UST-5813-5)

3) Main points of checking:

Check mechanical damage of contact terminal of connector.

EX.8 1) symptom:

Leakage of other parts of Ultrasound image.

2) Causes of failure:

Defect of Address control circuit (EP-393200)
Breakage of Probe cable
Failure of Probe

3) Main points of checking:

EP-393200 IC14 (CTRL1~CTRL8)

EX.9 1) symptom:

Bright vertical line runs sometimes in Ultrasound image area.

2) Causes of failure:

Delay time of transmitting or receiving is not stable.
(Defect of Delay line) (EP-393200)
Defect of Tx & Rx circuit (EP-393200)
Failure of Probe

3) Main points of checking:

EP-393200 TP12 (ECHO VIDEO)
EP-393200 TP3~TP10 (TRIG 1~TRIG 8)

EX.10 1) symptom:

Gain control dose not work

2) Causes of failure:

Defect of HIC (DHVD014) (EP-393200)
Defect of RV1~RV3

3) Main points of checking:

EP-393200 TP1,TP14 (US BLK,STC SIG)
USI-141 RV1~RV3

EX.11 1) symptom:

Black and white stripes are displayed in the Ultrasound image area, but image is not displayed

2) Causes of failure:

Defect of Transmission control circuit (EP-1895, EP-392800)
Defect of Freeze circuit (EP-392800)

3) Main points of checking:

EP-1895 IC9B 8 pin (FSYC)
IC9C 6 pin
EP-392800 IC2B 11 pin (TSYC/)
IC2E 11 pin (R CHG/)
IC2D 6 pin

EX.12 1) symptom:

Ultrasound image is not indicated in formation unless transmitting pulse is indicated on screen.

2) Causes of failure:

Ultrasound transmitting timing dose not correspond with memory address of image data.

3) Main points of checking:

EP-1895 IC8F 6 pin (FSTT)
EP-1894 J206 7 pin (FRST)

EX.13 1) symptom:

A portion of Ultrasound image area is flickering.

2) Causes of failure:

Defect of A/D Converter circuit (EP-1894)
Defect of Image memory (EP-1895)
Defect of Line interpolation circuit (EP-1895)

3) Main points of checking:

EP-1894 Data line of echo video data
EP-1895 Data line of echo video data
EP-1895 IC7G 11 pin (RAS/)
IC7G 8 pin (WE/)
IC7G 6 pin (CAS/)

TROUBLE OTHER THAN ULTRASOUND IMAGE

EX.14 1) Symptom: Freeze function is not effective

2) Causes of failure:

Defect of Freeze switch (EP-2241)
Defect of I/O Interface circuit (EP-392800)

3) Main points of checking:

EP-2241 S21
EP-392800 IC3E 9 pin (FZRQ)
IC2D 3 pin (FSYC)
IC2D 6 pin

EX.15 1) Symptom: Gray scale bar is not displayed on the screen

2) Causes of failure:

Defect of scale generator circuit (EP-1895)

3) Main points of checking:

EP-1895 IC5F 3 pin (GY0)
IC5F 2 pin (GY1)
IC5F 6 pin (GY2)
IC5F 7 pin (GY3)

EX.16 1) Symptom: Abnormal display of scale marker, ID code and caliper marker.

2) Causes of failure:

Defect of Graphic memory circuit (EP-392800)

3) Main points of checking:

EP-392800 IC4B 10 pin (ADDRESS SELECT)
IC1E 5 pin (GDT)

2-3-4. IP-0503-TV TROUBLESHOOTING

To employ this service manual:

1. Determine defective circuit by referring to Symptoms and Checkpoints.
2. Refer to checking procedure for the particular circuit to determine cause and correction.

CONTENTS

1. Symptoms and Checkpoints (Fig.1)
   a. No raster (see following page)
   b. Raster obtained, but no picture
   c. Blanking line visible
   d. Fuse opens (see following page)
   e. Both horizontal and vertical sync. Unstable
   f. Horizontal sync. Defective
   g. Vertical sync. Defective
   h. Raster becomes single horizontal line
   i. Raster becomes single vertical line
   j. Horizontal amplitude insufficient of excessive
   k. Vertical amplitude insufficient or linearity poor
   l. Picture out of focus
   m. Image small
   n. Upper portion of picture curved
   o. Jittering
   p. Ringing
   q. Video amplifier circuit
   r. Sync. Separator circuit

s. Vertical deflection circuit
t. Horizontal oscillator & drive circuit (AFC)
u. Horizontal output & high voltage circuit
v. CRT circuit
w. Back porch clamp circuit

No Raster (Fig.2)

a. Inspect horizontal oscillator & drive circuit
b. Check for drive waveform at TR13 base
c. Inspect output & high voltage circuit
d. CRT heater lighter?
e. Check for horizontal deflection pulse
f. Check for high voltage supply to CRT
g. CRT high voltage supply within specifications?
h. CRT defective.
i. Check for open fuse.

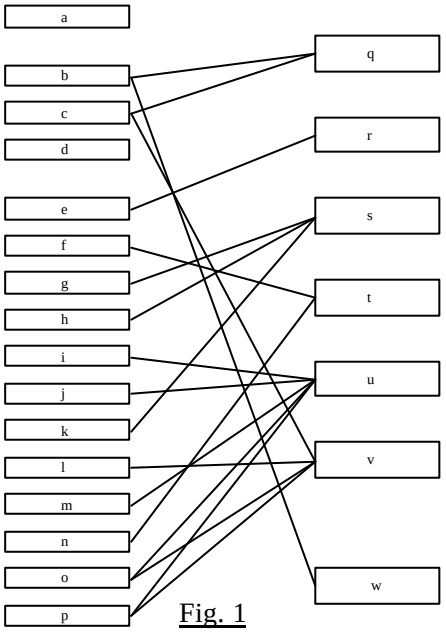


Fig. 1

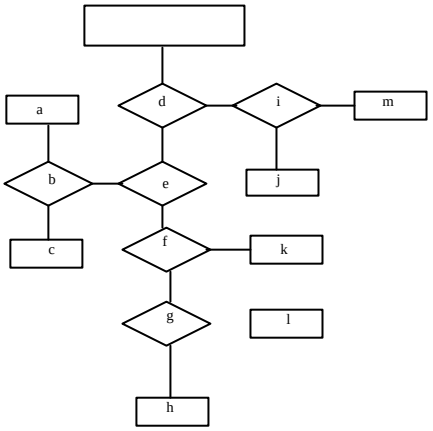


Fig. 2

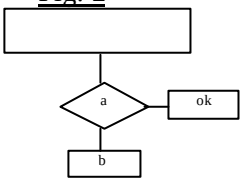


Fig. 3

j. Inspect power supply voltage
k. Inspect high voltage output circuit
l. Inspect CRT circuit
m. See following checking procedure (Fig. 3)

Fuse Opens (Fig.3)

a. Power supply voltage within specifications?
b. This type of defect is generally in horizontal output circuit.

2. Circuit Checking Procedure

1. Video Amplifier Circuit

Cause of malfunction can be easily determined by sequentially inspecting waveforms and voltages from first to last stage

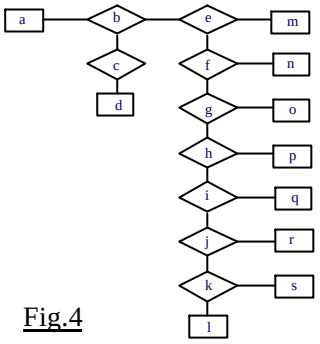


Fig.4

Fig. 4

a. No picture
b. Raster obtain
c. Voltage present at TR3 base? (2.0V~2.4V)
d. R13, R15 open: Inspect backporch clamp circuit.
e. Waveform present at TR3 collector?
f. Waveform present at TR3 base?
g. Waveform present at TR17 base?
h. Waveform present at TR18 emitter?
i. Waveform present at TR2 collector?
j. Waveform present at TR2 base?
k. Waveform present at TR1 base?
l. C1 open, R2 open.
m. R19 open.
n. TR3, TR4 defective.
o. R84 open, TR17 defective, C57 open.
p. R9, R81 open; C2, C56 open.
q. TR18 defective.
r. TR2 defective.
s. TR1 defective, R3, R4 open.

Blanking line visible

Inspect R58, R59, R60, R72, CD4, CD12, C55

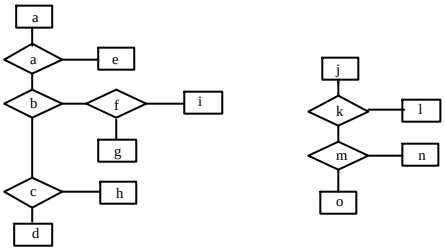
2. Sync. Separator Circuit

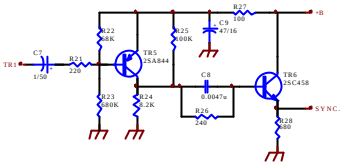
This circuit obtains sync. Components from composite video signal. Outputs are supplied to horizontal and vertical circuits. For this reason, such complaints as “both H & V sync. Absent” or “weak sync.” Are generally limited to this section. Determine the cause of malfunction is also relatively easy.

****

Unstable Sync. (Fig. 5)

a. Both horizontal and vertical sync. defective?
b. Vertical sync. defective?
c. Can single image be obtained by adjusting H.HOLD?
d. Inspect horizontal oscillator circuit.
e. Inspect sync. separator circuit.
f. By adjusting V.HOLD, dose picture roll upwards and downwards?
g. Inspect vertical oscillator circuit.
h. Inspect AFC circuit.
i. Inspect integrator circuit.





	Base	Collector	Emitter
TR5	1V	11V	11.8V
TR6	11V	11.9V	11V

Fig.5

Inspection Sequence Example:

j. Both H & V sync. absent.
k. Waveform present at TR6 base?
l. TR6 defective; R28, R29 open.
m. Waveform present at TR5 base?
n. TR5 defective; R24 R26 open.
o. C7 open; R21 open.

This circuit make brightness of block level fixed and get always stable video, not due to changes of contrast, when video signal would be input.

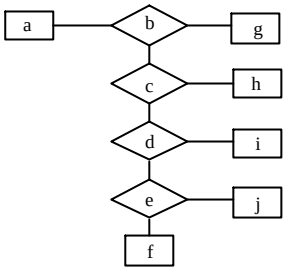


Fig.6

Fig. 6

a. No picture and No raster
b. Voltage present at TR9 collector? (2.0V~2.4V)
c. Waveform present at TR9 base?
d. Waveform present at TR8 base?
e. Waveform present at TR7 base?
f. R29, C10 open.
g. Inspect video amplifier circuit.
h. TR9 defective.
i. TR8 defective. R36, C15 open.
j. TR7 defective. R31, C12 open.

4. Vertical Deflection Circuit (Fig. 7)

(1). Raster becomes single horizontal line.

This symptom occurs when sawtooth wave current is not applied to deflection coil. Inspect circumferential parts of IC and opened resistor and shorted or opened condenser.

(2). Insufficient vertical amplitude.

Symptom produced when amplitude of sawtooth wave current in vertical deflection coil is insufficient. IC, RV3 defective and Inspect circumferential parts.

(3). Vertical Linearity Poor.

This symptom is produced by insufficient linearity of sawtooth wave current in deflection coil.

a. Current b. Picture
c. Bottom d. Center
e. Top

(A) Correct (B) Bottom of picture contracts

© Top of picture contracts

f. Poor vertical linearity

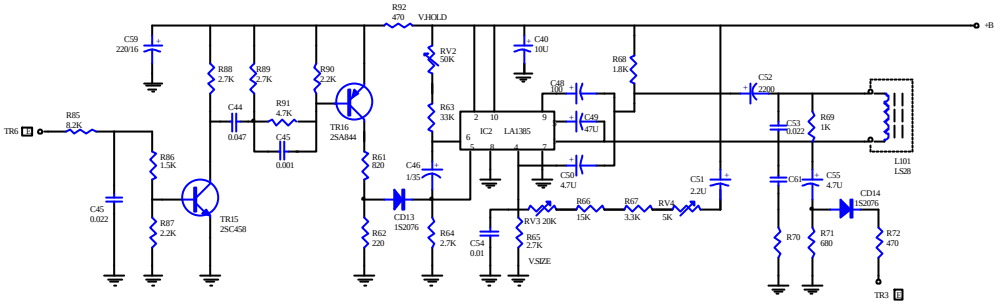
g. Does linearity change with V.LIN VR(RV4) adjustment?

h. Is picture affected by V.HEIGHT VR(RV3) adjustment?

i. IC defective.

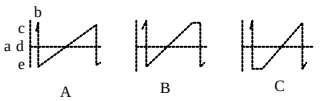
j. Inspect C50, C51, jR67, RV4.

k.Inspect C47, R65, R66, RV3.



	Base	Collector	Emitter
TR15	0.7V	12V	0V
TR16	2V	12V	0V

1	2	3	4	5
12V	11.9V	12V	6V	4V
6	7	8	9	10
3V	1.2V	0V	1.2V	11.9V



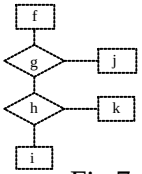


Fig.7

5. Horizontal Oscillator & Drive Circuit (AFC) (Fig.8)

(1) Horizontal Sync. Breakup

Turning the H.HOLD control can provide an indication of the type of malfunction.

a. Phase discriminator circuit
b. Horizontal Oscillator Circuit
c. Single picture can be obtained with difficulty, then slips horizontally.
d. Number of horizontal lines numerous can be reduced, but single picture not obtained.
e. Horizontal lines numerous and picture completely unobtainable.
f. Slanted lines from right downward indicate oscillator frequency too high.
g. Slanted lines from left downward indicate oscillator frequency too low.
h. Horizontal sync. Breakup
i. Comparator waveform (B) applied to phase discriminator?
j. Does point (A) potential vary with variation of L1?
k. Oscillator circuit defective.
l. Inspect C22, C23, R57, FBT
m. Phase discriminator circuit defective; inspect R56, CD5, CD6, TR10.

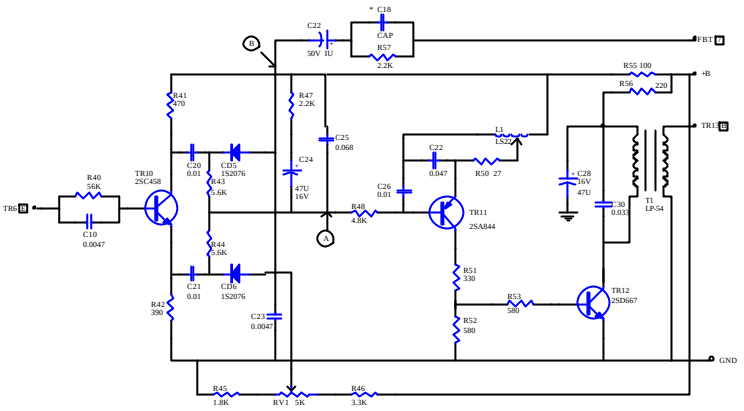
Determining oscillator circuit multifunction:
Observe direction of slanted lines to determine high or low oscillator frequency.
1. If oscillator frequency is high, inspect components which raise oscillator transistor(TR11) base potential.
2. If oscillator frequency is low, inspect components which lower oscillator transistor(TR11) base potential.

If AFC smoothing circuit (C24, C25, R47) in phase discriminator circuit output is defective, wavy picture or unstable horizontal sync. Can be produced.

(2) No raster (Horizontal oscillation stopped)

This symptom develops when horizontal drive pulse is not applied to horizontal output transistor base. Difficulty can be determined by tracing the waveform.

Check procedure
n. Horizontal oscillation stopped.
o. Waveform present at TR12 collector?
p. Waveform present at TR12 base?
q. Waveform present at TR11 collector?
r. Inspect TR4, L1, R56, R52.
s. Inspect from drive transformer to H.OUT TR base.
t. Inspect R56, T1, TR12, C30.
u. R53 open.



	BASE	COLLECTOR	EMITTER
TR10	9Vp-p (-3.4V)	6.5 Vp-p (10.5V)	4.0 Vp-p (0.5V)
TR11	4Vp-p (10.9V)	9 Vp-p (1.3V)	2.5 Vp-p (11V)
TR12	0.6Vp-p (0.3V)	5.2 Vp-p (3.2V)	(0V)

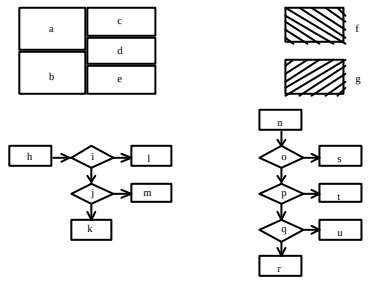


Fig. 8

6. Horizontal Output Circuit and High Voltage Circuit (Fig.9)

Malfunctions which can be attributed to this circuit are:

(1). No raster

This symptom occurs when high voltage is not applied to CRT. Possible causes are deflection pulse not applied to flyback transformer primary or defective flyback transformer or high voltage rectifier.

(2). Fuse open when power or high voltage rectifier.

This symptom is caused by excessive +B current due to defects of following components.

TR13 C-E short, CD9 short

C31,C32,C36 short

Check with VOM

FBT short

(3). Horizontal deflection stopped (vertical line produced)

This occurs when sawtooth wave current is nit applied to deflection yoke. Suggested checkpoints are open L2,L3,L101.

(4). In the case that ringing and jittering cause:

It is phenomenon that vertical line is found on lower part (on left side) and/or a little noise cause. CDLL and/or flyback transformer (FBT) might be broken.

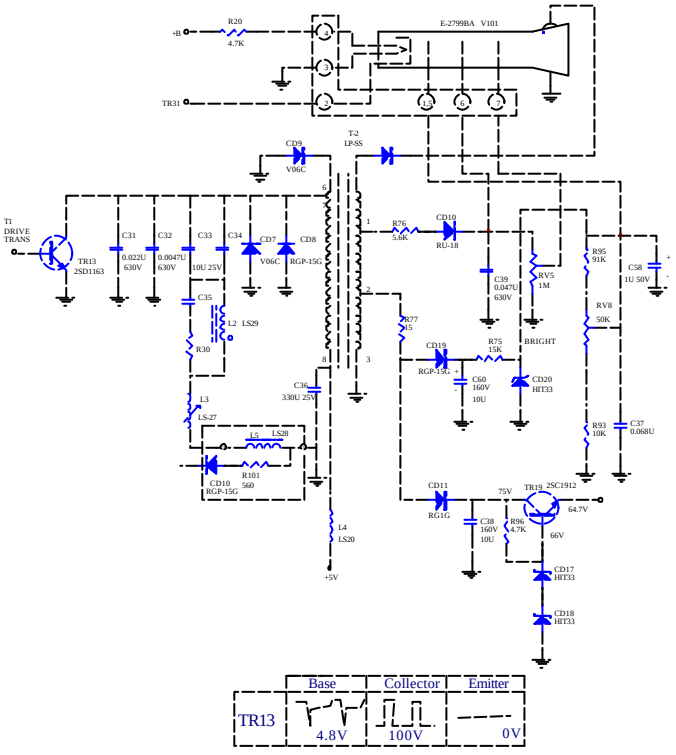


Fig.9

7. CRT Circuit (Fig.9)

Main problems affecting this circuit are abnormal power supply to CRT and defective CRT. Malfunction are easily determined due to the small number of parts.

(1). No raster (normal high voltage supplied to CRT)

Observe if heater is glowing. If heater does not glow, inspect open R20 and for possible open heater.

(2). Brightness does not vary when BRIGHTNESS control is rotated,

This occurs when cathode potential is not varied by BRIGHTESS control rotation. Possible causes are R75, open RV6, RV102 defective.

MAINTENANCE:

(1). Cleaning on Picture Tube

As Picture Tube is always apt to adhere dusts in air because static electricity rise, and also the resolution would therefore be lowered, please keep cleaning periodically.

(2). Caution on Checking:

It is necessary for you to take care in its treating, because transistor is very weak in electric shock and is suddenly broken when voltage over at rated is put on.

As especially Horizontal Circuit is of high power-electric-circuit, and as a little abnormal of handling cause some times transistor broken, please do not check high voltage caused by means of making spark with screw driver, etc.

If such tester would not be available, while removing CRT Socket, please check cause of high voltage removing connector after putting on connector and after discharge voltage charged in CRT by means of nearing lead-wire which is on earth to Anode of CRT.

MANUAL:

Operation of Adjustment-Buttons on the printed circuit board

H. HOLD (RV1) : When the picture is offset, or slanting stripes and bars appear, adjust "H. HOLD" control.

V. HOLD (RV2) : When the picture is overlapped or rolling up or down, adjust "H. HOLD" control.

CONTRAST (RV7): When the picture contrast is too weak or too strong, adjust "CONT." control.

BRIGHTNESS (RV8): When the picture contrast is too bright or too dark, adjust "BRIGHT." control.

V. LIN (RV4): When the pattern is distorted at the top or bottom, adjust "VV.LIN." control.

V. HEIGHT (RV3): When the center circle of the pattern is eggy, adjust "V.HEIGHT." control.

H. RRO (L1): When the pattern is offset, or stripes and bars appear and cannot be corrected with Hold control, adjust "H. RRO." Control

FOCUS (RV5): When the pattern is blurred or out of focus, adjust "FOCUS" control.

SECTION 3. PARTS LIST

USI-141 MECHANICAL PARTS LIST

NO	PARTS	TYPE AND DESCRIPTION	NUMBER	REFERENCE
1.1	Monitor PCB Unit	PC-0017N（NTSC）	1	NTSC
1.2	Monitor PCB Unit	PC-0017P（PAL)	1	PAL
2	CRT(include coil）	C5M13P4GH	1	
3	Power PCB Unit	EP-1882G	1	
4	A/D&D/A PCB Unit	EP-1894-7	1	
5	DSC PCB Unit	EP-1895E-6	1	
6.1	MPU PCB Unit (NTSC)	EP392801	1	AAV(NTSC)
6.2	MPU PCB Unit (PAL)	EP392800	1	PAL
7	RX/TX PCB Unit	EP-393200A	1	
8	KEY Unit	EP-2241	1	
9.1	Power transformer（include connector）	R65-02-7-1(120V)	1	AAV(NTSC)
9.2	Power transformer（include connector）	R65-95-3-2(220V)	1	PAL
10	Fuse (100V)用	T 1A 250V	1	
11	Probe (include PCB)	UST-5813-5	1	
12	PANEL	MM179205U	1	
13	BOTTEM	MM102779	1	
14	UPPER COVER(include handle）	MM102510	1	

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